DERWENT-ACC-NO: 1997-219025

DERWENT-WEEK: 199720

TITLE: Solar battery module - has diode element to which deposit formation of ip- type bypass diode with silicon type non-monocrystal semiconductor is done on electrically conductive substrate

PRIORITY-DATA: 1995JP-0220943 (August 29, 1995)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 09064397 A	March 7, 1997	N/A	020	H01L 031/042

INT-CL (IPC): H01L029/861, H01L031/04 , H01L031/042

ABSTRACTED-PUB-NO: JP 09064397A

BASIC-ABSTRACT:

The module has a p type, n type and i type semiconductor layers which form a pin junction on an electrically conductive substrate of multilayered tandem type solar cell.

A deposit formation of ip- type bypass diode with silicon type non-monocrystal semiconductor is done on a diode element (102) of ip- type on the electrically conductive substrate.

ADVANTAGE - Prevents short circuit generation by partial optical interruption due to high degree of humidity.

PAT-NO: JP409064397A

DOCUMENT-IDENTIFIER: JP 09064397 A

TITLE: SOLAR CELL AND SOLAR CELL MODULE

PUBN-DATE: March 7, 1997

INVENTOR-INFORMATION:
NAME
FUJIOKA, YASUSHI

INT-CL (IPC): H01L031/042, H01L029/861 , H01L031/04

US-CL-CURRENT: 257/E27.123

ABSTRACT:

PROBLEM TO BE SOLVED: To restrain the short circuit of a solar cell module from being generated when light is shut off partly at high humidity by a method wherein a bypass diode is used as an i-n or i-p junction diode element which is deposited and formed on a conductive substrate and which is composed of a silicon non-single- crystal semiconductor.

SOLUTION: Since a semiconductor layer at a solar cell element 101 and a semiconductor layer at a diode element 102 are composed of a silicon non-single crystal of the same quality, the semiconductor layers are formed

simultaneously on a conductive substrate. Since a direction toward a collector electrode 108D from the conductive substrate 103 in the diode element 102 is a forward direction (or a reverse direction), the diode element 102 is parallel-connected to the solar cell element 101 in the reverse direction when the collector electrode 108 at the solar cell element 101 and the collector electrode 108D at the diode element are connected by a conductor 109, and the diode element acts as a bypass diode. Thereby, even when light is shut off partly in the array of tandem solar cell elements, a reverse voltage which is applied to a light-shielding element becomes low, and the short circuit of the element can be suppressed.

(19)日本国特許庁（JP）　(12)公開特許公報(A)　(11)特許出願公開番号
特開平9－64397
(43)公開日　平成9年(1997)3月7日

(51)Int.Cl.*	識別記号	庁内整理番号	FI		技術表示箇所
H01L 31/042			H01L 31/04	R	
29/861			29/91	E	
31/04			31/04	W	

審査請求　未請求　請求項の数4　OL　(全 20 頁)

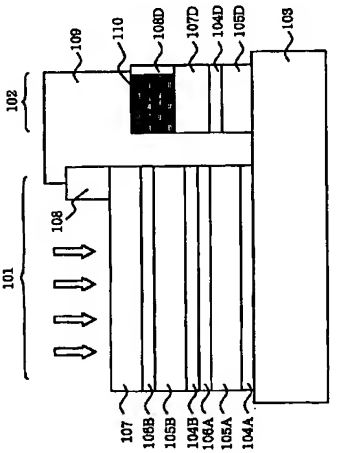
(21)出願番号　特願平7－220943

(22)出願日　平成7年(1995)8月29日

(71)出願人　000001007
キヤノン株式会社
東京都大田区下丸子3丁目30番2号
(72)発明者　藤岡　靖
東京都大田区下丸子3丁目30番2号キヤノン株式会社内
(74)代理人　弁理士　福森　久夫

(54)【発明の名称】　太陽電池および太陽電池モジュール

(57)【要約】
【課題】　高温度下での部分的な光遮断による太陽電池モジュールの短絡の発生を抑制し、信頼性の高い太陽電池及び太陽電池モジュールを提供する。
【解決手段】　本発明の太陽電池は、n型半導体をn、i型半導体をi、及びp型半導体をpとした場合、導電性基板上にシリコン系非単結晶半導体からなるnipまたはpinまたはpin接合を複数積層したタンデム型太陽電池素子と、前記太陽電池素子とは電気的に逆方向となるように、前記太陽電池素子と並列接続されたバイパスダイオードからなる太陽電池において、前記バイパスダイオードが、前記導電性基板上に堆積形成されたシリコン系非単結晶半導体からなるinまたはip接合のダイオード素子であることを特徴とする。また、本発明の太陽電池モジュールは、上記太陽電池を複数個直列接続したことを特徴とする。



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【特許請求の範囲】

【請求項1】　n型半導体をn、i型半導体をi、及びp型半導体をpとした場合、導電性基板上にシリコン系非単結晶半導体からなるｎｉｐまたはｐｉｎ接合を複数積層したタンデム型太陽電池素子と、

前記太陽電池素子とは電気的に逆方向となるように、前記太陽電池素子と並列接続されたバイパスダイオードからなる太陽電池において、

前記バイパスダイオードが、前記導電性基板上に堆積形成されたシリコン系非単結晶半導体からなるｉｎまたはｉｐ接合のダイオード素子であることを特徴とする太陽電池。

【請求項2】　前記ダイオード素子におけるｉは、非晶質シリコンゲルマニウムからなることを特徴とする請求項1に記載の太陽電池。

【請求項3】　前記バイパスダイオードとは電気的に順方向となるように、前記バイパスダイオードと並列接続された単結晶半導体からなるダイオードを有することを特徴とする請求項1又は2に記載の太陽電池。

【請求項4】　請求項1乃至3の少なくとも1項に記載の太陽電池を、複数個直列接続したことを特徴とする太陽電池モジュール。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、太陽電池および太陽電池モジュールに係る。より詳細には、太陽電池素子とは電気的に逆方向となるように、太陽電池素子と並列接続されたバイパスダイオードを設けた太陽電池および太陽電池モジュールに関する。

【0002】

【従来の技術】現在、電力用太陽電池は一般的に複数の太陽電池素子を直列接続した素子アレイの形でモジュール化されている。

【0003】直列接続で動作する場合、素子アレイの一部の素子が影に入ると、影になった素子にその他の発電している素子の発生電圧の合計が逆方向電圧の形で印加され、この逆方向電圧が素子の耐圧を超える値になると素子の破壊が生じるという問題がある。

【0004】このような部分的な光遮断による素子の破壊を防止する方法としては、直列接続された各素子に逆向きにいわゆるバイパスダイオードを並列に接続する方法が知られており、一般的に行われている。また、バイパスダイオードを光起電力素子と同時に形成することも行われており、非単結晶半導体を用いた太陽電池においても、バイパスダイオードを同一基板上に形成する技術がいくつか提案されている。

【0005】特公昭63－13358号公報には、絶縁基板上に堆積した非晶質シリコンを用いた太陽電池で、素子の一部を分離して逆向きに電極接続し、バイパスダイオードを形成する技術が開示されている。特公平2－

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5575号公報には、同一基板上に非晶質シリコン太陽電池とショットキー障壁ダイオードを分離形成する技術が開示されている。

【0006】このように各太陽電池素子にバイパスダイオードを並列接続すれば、素子アレイの一部の素子が影になった場合においても、影になった素子にはバイパスダイオードの順方向電圧以上の逆方向電圧は印加されず、高電圧印加による太陽電池素子の破壊を防ぐことができる。

【0007】ところが、このようにバイパスダイオードを接続していても、一定の条件の下では部分的に影になった太陽電池素子が短絡状態になることがありうる。

【0008】すなわち、バイパスダイオードの順方向電圧は単結晶シリコンのｐｎ接合ダイオードの場合約0.8V程度で、部分的に光遮断された太陽電池素子にはこの程度の逆方向電圧は印加される。通常、この程度の電圧では非晶質シリコン太陽電池素子には短絡を生じないが、太陽電池素子の電極や裏面反射膜としてイオン化して移動しやすい金属を用いた場合、太陽電池素子の半導体膜に膜の端部やクラック、ピンホール等を介して水分が侵入した状態においては、この程度の電圧でも金属イオンが半導体膜中を移動し、半導体膜に部分的な導電路を形成し、短絡電路を発生させるため、危険な状態が生じるという問題がある。

【0009】以下では、導電性基板上に裏面の光反射層として反射率の高いＡｇの層を形成し、その上に非晶質Ｓｉのｎ，ｉ，ｐ型半導体層をこの順に積層し、さらにその上に透明電極を形成した太陽電池素子の場合を取り上げ、上記問題に関してより具体的に説明する。

【0010】非単結晶シリコン系半導体を用いた太陽電池においては、光入射側にｐ型半導体層を配置するｎｉｐ接合構造が主流であり、入射光を有効利用して発生電流量を増加させるために半導体層を一度透過した光を裏面で反射させる裏面光反射層の形成することも多く行われており、この例は極めて一般的な太陽電池素子の構成である。

【0011】このような太陽電池素子で、通常発電時の全面に光照射がなされた状態では、導電性基板側が負の電圧を発生するため、半導体層に水分が侵入して光反射層のＡｇの一部が正イオン化しても半導体膜中をＡｇイオンが移動することはない。

【0012】ところが、このような太陽電池で半導体膜中に水分が侵入した状態で、該太陽電池素子が素子アレーの中で部分的に光遮断された場合には、透明電極側に負の電圧が印加されると、光反射層のＡｇの一部が正イオン化し、正のＡｇイオンが半導体膜中を負の電圧の印加された透明電極に向かって移動し、透明電極側で再びＡｇとして析出することが考えられる。これにより、半導体膜中に部分的なＡｇの短絡電路が形成される危険性が高い。

【0013】このような金属イオンのイオン化、移動、析出の現象は単結晶シリコンのｐｎ接合ダイオードの約０．８Ｖの順方向電圧でも発生し、印加される電圧にほぼ比例して進行するものと考えられるが、この現象が一定以上進行すると半導体膜に短絡電路が形成され、短絡電流が急激に増加するものと考えられる。

【0014】このような現象は、半導体膜裏面にイオン化するような金属を使わないこと、あるいは水蒸気等の水分の侵入を完全に防ぐことができれば回避できる。

【0015】しかし、集電電極や裏面反射層としては高導電性、高反射率の金属を使用する必要があり、このような金属として多く用いられる銀、銅等の金属はイオン化しやすい傾向がある。

【0016】また、電力用太陽電池として長年にわたって屋外の厳しい環境条件で使用する場合、モジュールに完璧な防水を保証することは極めて困難であり、太陽電池素子全体を完全にガラスで封止する等の防水対策を行うとモジュールの重量が非常に重くなり、設置方法が限定される。また、電力用として商用電力と同等の発電コストを得るにはコストがかかりすぎるという問題も生じる。

【0017】前記の特公昭６３－１３３５８号公報に開示された、非晶質シリコンを用いた太陽電池を絶縁基板上に堆積し、素子の一部を分離して逆向きに電極接続してバイパスダイオードを形成する方法では、非晶質シリコンのｐｉｎ接合からなる光起電力素子の順方向電圧は約１．０Ｖで、単結晶シリコンのｐｎ接合からなるダイオードの順方向電圧と同等で、単結晶シリコンダイオードにかえて採用しても前述の高湿下の部分的光遮断による半導体膜の短絡の発生を抑制するには効果がない。特に、太陽電池素子が複数のｎｉｐ接合を積層したタンデム型構造の場合には、太陽電池素子の開放電圧が高いため、バイパスダイオードの順方向電圧が太陽電池素子の開放電圧に比例してかなり高くなるという問題がある。

【0018】一方、前記の特公平２－５５７５号公報に開示された、同一基板上に非晶質シリコン太陽電池とショットキー障壁ダイオードを形成する方法では、ショットキー障壁ダイオードの順方向電圧はｐｎ接合ダイオードの順方向電圧よりも低いため、単結晶シリコンのｐｎ接合ダイオードにかえて採用すれば高湿下の部分的光遮断による短絡の抑制に効果があるものと考えられる。

【0019】しかし、前記の特公平２－５５７５号公報に開示された方法では、同一の導電性基板上に太陽電池素子とダイオードを形成した場合、導電性基板上に絶縁層を設けて太陽電池素子とダイオードの電極を完全に分離しない限り、導電性基板に対して太陽電池素子とダイオードが同方向の極性になるため、太陽電池素子にダイオードを逆方向に並列接続することができず、逆流防止のブロッキングダイオードとして使用することはできるものの、バイパスダイオードとしては使用できないという問題があった。

【0020】

【発明が解決しようとする課題】本発明は、高湿度下での部分的な光遮断による太陽電池モジュールの短絡の発生を抑制し、信頼性の高い太陽電池及び太陽電池モジュールを提供することを目的とする。

【0021】

【課題を解決するための手段】本発明の太陽電池は、ｎ型半導体をｎ、ｉ型半導体をｉ、及びｐ型半導体をｐとした場合、導電性基板上にシリコン系非単結晶半導体からなるｎｉｐまたはｐｉｎ接合を複数積層したタンデム型太陽電池素子と、前記太陽電池素子とは電気的に逆方向となるように、前記太陽電池素子と並列接続されたバイパスダイオードからなる太陽電池において、前記バイパスダイオードが、前記導電性基板上に堆積形成されたシリコン系非単結晶半導体からなるｉｎまたはｉｐ接合のダイオード素子であることを特徴とする。

【0022】また、前記ダイオード素子におけるｉは、非晶質シリコンゲルマニウムからなることが好ましい。

【0023】さらに、前記バイパスダイオードとは電気的に順方向となるように、前記バイパスダイオードと並列接続された単結晶半導体からなるダイオードを有することが望ましい。

【0024】本発明の太陽電池モジュールは、上述した太陽電池を、複数個直列接続したことを特徴とする。

【0025】

【作用】請求項１に係る発明では、ｎ型半導体をｎ、ｉ型半導体をｉ、及びｐ型半導体をｐとした場合、導電性基板上にシリコン系非単結晶半導体からなるｎｉｐまたはｐｉｎ接合を複数積層したタンデム型太陽電池素子と、前記太陽電池素子とは電気的に逆方向となるように、前記太陽電池素子と並列接続されたバイパスダイオードからなる太陽電池において、前記バイパスダイオードが、前記導電性基板上に堆積形成されたシリコン系非単結晶半導体からなるｉｎまたはｉｐ接合のダイオード素子であるため、前記導電性基板上に絶縁層を設けて、前記太陽電池素子と前記バイパスダイオードの電極を完全に分離する必要がなく、かつ、ｐｉｎまたはｎｉｐ接合のダイオード素子と比較して、ダイオード素子の順方向電圧を約半分の０．４５～０．５Ｖとすることができる。

【0026】請求項２に係る発明では、前記ダイオード素子におけるｉを非晶質シリコンゲルマニウムとしたため、バンドギャップの狭いａ－ＳｉＧｅをｉ型半導体層に用いた場合には順方向電圧は更に低くなり、ＳｉとＧｅの組成比にもよるが、約０．３Ｖ程度にまで下げることができる。

【0027】請求項３に係る発明では、前記バイパスダイオードとは電気的に順方向となるように、前記バイパスダイオードと並列接続された単結晶半導体からなるダ

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イオードを有するため、バイパスダイオードの順方向電圧の引き下げと許容電流容量の増大の両立を図ることができる。

【0028】上述した請求項1～3による順方向電圧の低減は、タンデム型太陽電池素子のアレーに部分的な光遮断が生じても遮光素子に印加される逆方向電圧のさらなる低下をもたらす。

【0029】その結果、高電圧による素子の絶縁破壊はもとより、太陽電池素子の半薄体膜に水分が侵入した場合においても金属イオンの移動による素子の短絡が大幅に抑制することが可能な太陽電池が得られる。

【0030】請求項4に係る発明では、請求項1～3の少なくとも1項に記載の太陽電池を、複数個直列接続したため、高湿度下での部分的な光遮断による太陽電池モジュールの短絡の発生が抑制される。その結果、信頼性の高い太陽電池モジュールが得られる。

【0031】

【発明の実施の形態】

（太陽電池）本発明に係る太陽電池は、基本的には、導電性基板と、複数のｎｉｐ（またはｐｉｎ）接合からなるタンデム型太陽電池素子と、ｉｎ（またはｉｐ）接合からなるダイオード素子から構成されたものである。実際には、ｎｉｐ（またはｐｉｎ）接合の重なる数、及び太陽電池素子とダイオード素子の配置関係から、次に示す多数の太陽電池が考えられる。

【0032】以下では、図面を参照しながら、本発明に係る太陽電池に関して詳細に説明する。

（太陽電池ａ）図1は、本発明に係る太陽電池の一例を示す模式的断面図であり、以後太陽電池ａと呼称する。太陽電池ａとは、太陽電池素子とダイオード素子が導電性基板の同一面上にあり、太陽電池素子とダイオード素子が導電性基板と導線を介してのみ電気的に接続されている場合である。

【0033】図1において、太陽電池素子１０１は導電性基板１０３上にｎ（またはｐ）型半導体層１０４Ａ、実質的に真性な半導体層１０５Ａ、ｐ（またはｎ）型半導体層１０６Ａ、ｎ（またはｐ）型半導体層１０４Ｂ、実質的に真性の半導体層１０５Ｂ、ｐ（またはｎ）型半導体層１０６Ｂ、透明電極１０７、集電電極１０８から構成されている。

【0034】また、ダイオード素子１０２は太陽電池素子と同一の導電性基板１０３上に形成され、実質的に真性の半導体層１０５Ｄ、ｎ（またはｐ）型半導体層１０４Ｄ、透明電極１０７Ｄ、集電電極１０８Ｄから構成されている。

【0035】透明電極側からの光入射によって、太陽電池素子１０１には導電性基板１０３側が負（または正）で、上部集電電極１０８側が正（または負）の向きの起電力が発生する。

【0036】一方、ダイオード素子１０２には遮光塗料

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１１０等により遮光されており、半導体層への光入射は行われず、光起電力は発生しない。ダイオード素子１０２は、導電性基板１０３から集電電極１０８Ｄへの向きが順方向（または逆方向）であるため、太陽電池素子１０１の集電電極１０８とダイオード素子の集電電極１０８Ｄとを導線１０９で接続することによって、ダイオード素子１０２は太陽電池素子１０１に逆方向に並列接続され、バイパスダイオードとして作用する。

【0037】本発明において、太陽電池素子はタンデム型の構造を有するため、高い電圧を発生する。半導体層としてアモルファスシリコン系材料を用いた場合、ｉ型層がａ－Ｓｉ／ａ－Ｓｉのｎｉｐｎｉｐ２層タンデム型素子で約１．８Ｖ、ａ－Ｓｉ／ａ－Ｓｉ／ａ－ＳｉＧｅのｎｉｐｎｉｐｎｉｐ３層タンデム型素子で約２．６Ｖの高い開放電圧が発生する。

【0038】しかし、本発明のバイパスダイオード素子は単独のｉｎまたはｉｐ接合構造であるため、その順方向電圧は単独のｐｉｎまたはｎｉｐ接合ダイオードの順方向電圧の約半分になる。本発明のバイパスダイオード素子の順方向電圧は、単結晶シリコンのｐｎ接合からなるダイオードの順方向電圧よりも低く、ｉ型半導体層がａ－Ｓｉの場合は約０．４５～０．５Ｖになる。また、バンドギャップの狭いａ－ＳｉＧｅをｉ型半導体層に用いた場合には順方向電圧は更に低くなり、ＳｉとＧｅの組成比にもよるが約０．３Ｖ程度にまで下げることができる。

【0039】この低い順方向電圧のため、タンデム型太陽電池素子のアレーに部分的な光遮断が生じても遮光素子に印加される逆方向電圧が非常に低くなり、高電圧による素子の絶縁破壊はもとより、太陽電池素子の半薄体膜に水分が侵入した場合においても金属イオンの移動による素子の短絡が大幅に抑制される。

【0040】本発明において、ダイオード素子の半導体膜上にはＩＴＯ（$In_2O_3+SnO_2$），SnO_2，In_2O_3，ＺｎＯ等の透明電極を積層することが望ましい。図1において、ダイオード素子１０２の半導体層１０４Ｄ上に集電電極１０８Ｄを直接設けず、光照射しないにもかかわらず透明電極１０７Ｄを積層しているのは、ダイオード素子の集電電極１０８Ｄの金属が太陽電池素子の発電電圧で半導体膜へ侵入することを阻止し、ダイオード素子の短絡を防止するためである。

【0041】本発明において、太陽電池素子の半導体層とダイオード素子の半導体層は同質のシリコン系非単結晶からなるため、導電性基板上に同時に形成することが可能である。図1において太陽電池素子１０１とダイオード素子１０２の半導体膜は導電性基板１０３上で分離されているが、ダイオード素子のｉ型層１０５Ｄは太陽電池素子のｉ型層１０５Ａと同時に、ｎ（ｐ）型層１０４Ｄは１０４Ｂと同時に、透明導電膜１０７Ｄは１０７と同時に、集電電極１０８Ｄは１０８と同時に堆積形成

することができる。その場合、ダイオード素子の部分に太陽電池素子の堆積膜の一部を堆積させるには、マスキング等の公知の手段を用いることができる。太陽電池素子でダイオード素子で必要な膜以外の膜を堆積する際に、ダイオード素子形成領域をマスクで覆って膜が堆積されない様にすることで所望の膜だけを選択して堆積することができる。

【0042】（太陽電池b）図2は、本発明に係る太陽電池の一例を示す模式的断面図であり、以後太陽電池bと呼称する。太陽電池bとは、ダイオード素子として堆積する半導体膜を、太陽電池素子と分離することなく連続して堆積した場合である。

【0043】図2における201～210は、図1の101～110に対応している。図2において、ダイオード素子202のi型層205A、n（p）型層204Bは太陽電池素子201のi型層205A、n（p）型層204Bと連続している。

【0044】半導体層を共用することで該半導体層には横方向に漏れ電流が生じるが、非単結晶シリコン膜の抵抗率はかなり高く、膜厚も薄いため該半導体層における横方向への漏れ電流は極めて小さく、導電率の高い透明電極と集電電極さえ数mm程度分離すれば、太陽電池素子の特性には実用上悪影響を及ぼさない。共用する半導体層には太陽電池素子201の端部で段差ができるが、ここで膜が連続している必要はなく、段差で切断されていた方が太陽電池素子とダイオード素子との間隔が狭くても横方向への漏れ電流を防止できる点でより望ましい。

【0045】なお、太陽電池素子とダイオード素子の間の領域は、光が照射されると太陽電池素子とは逆方向の光起電力を発生するため、上部電極がなく殆ど集電されないものの、遮光塗料210等を塗布するなどして遮光することが望ましい。

【0046】（太陽電池c）図3は、本発明に係る太陽電池の一例を示す模式的断面図であり、以後太陽電池cと呼称する。太陽電池cとは、導電性基板を介して、太陽電池素子とダイオード素子を設けた場合である。図3における301～309は、図1の101～109に対応している。

【0047】この場合、ダイオード素子302は導電性基板301の光照射裏面に形成されるので、ダイオード素子の形成によって太陽電池モジュールの受光面積が減少することがない。また、ダイオード素子を受光面積の減少を気にせず大面積に形成することが可能で、ダイオード素子の電流容量を大きくとることができる。さらに、ダイオード素子が導電性基板によって遮光されるため、ダイオード素子を遮光塗料等で遮光する必要がないという利点がある。

【0048】なお、この場合、ダイオード素子302の半導体層305D、304Dは、太陽電池素子301の半導体層305A，304Bの堆積時に導電性基板303の裏面にも同時に半導体膜を堆積することによって容易に形成することができる。

【0049】また、図3ではダイオード素子は導電性基板の裏面にのみ形成されているが、裏面と表面の両面に形成してもよい。

【0050】（太陽電池d）図4は、本発明に係る太陽電池の一例を示す模式的断面図であり、以後太陽電池dと呼称する。太陽電池dとは、図1の太陽電池aに、単結晶半導体からなるダイオード411をさらに並列接続して設けた場合である。図4における401～409は、図1の101～109に対応している。

【0051】前述したように、太陽電池素子401には同一基板403上にダイオード素子402が形成され、導線409で逆方向に並列接続されており、太陽電池アレイ化された場合、単結晶ダイオード411がなくともバイパスダイオードとして作用する。

【0052】このとき、ダイオード素子402の順方向電圧が低いため、太陽電池アレイに部分的な光遮断が生じても太陽電池素子401に印加される逆方向電圧はかなり低くなる。

【0053】ところが、ダイオード素子402は太陽電池素子401と同一の基板403上にあり、受光面積の減少を防ぐために太陽電池素子401に比較してダイオード素子402の面積はあまり大きくできない。そのため、単結晶ダイオード411がない場合、太陽電池アレイで部分的な光遮断が生じた場合には、小さなダイオード素子402に太陽電池素子401の発生電流にはぼ等しい太陽電池アレイの他の太陽電池素子の発生電流が順方向電流として流れることになり、この順方向電流がシリコン系非単結晶半導体からなるダイオード素子402の許容電流容量を超えるとダイオード素子402破壊される危険性がある。

【0054】順方向電圧は高くでも、電流容量の大きな単結晶ダイオード411をダイオード素子402に同方向に並列に接続した場合、印加電圧の高い領域での大電流は単結晶ダイオード411を流れ、単結晶ダイオードの順方向電圧より印加電圧の低い領域での小電流は非単結晶半導体からなるダイオード素子402を流れるように作用し、バイパスダイオードの順方向電圧の引き下げと許容電流容量の増大の両立が図られる。

【0055】なお、本発明において用いられる単結晶ダイオードとしては、シリコンまたはゲルマニウムからなり、pn接合、pin接合またはショットキー障壁接合構造を有する個別のダイオード素子が挙げられる。該単結晶ダイオードの順方向許容電流容量（最大定格値）は、望ましくは各太陽電池素子のAM1．5（1000W／m²）照射時の短絡電流の2倍以上、より好ましくは3倍以上とする。

【0056】（太陽電池e～h）図6～図9は、本発明

に係る太陽電池の一例を示す模式的断面図であり、以後太陽電池e～hと呼称する。太陽電池e～hは、ｎｉｐまたはｐｉｎ接合を３個積層した３層タンデム型太陽電池素子を用いた場合である。

【００５７】この場合には、太陽電池素子と同一基板上に形成するダイオード素子に用いる半導体層を、太陽電池素子のどの半導体層と同時に形成するかで複数の組み合わせが存在する。

【００５８】図６～図９では、太陽電池素子のどの半導体層とダイオード素子の半導体層が同時に形成されたかが分かるように、半導体層が連続して示してある。

【００５９】図６（太陽電池ｅ）は、ダイオード素子の半導体層を、下から順に、太陽電池素子の第１層目のセルのｉ型半導体層、第２層目のセルのｎ（またはｐ）型半導体層、とした場合である。

【００６０】図７（太陽電池ｆ）は、ダイオード素子の半導体層を、下から順に、太陽電池素子の第２層目のセルのｉ型半導体層、第３層目のセルのｎ（またはｐ）型半導体層、とした場合である。

【００６１】図８（太陽電池ｇ）は、ダイオード素子の半導体層を、下から順に、太陽電池素子の第１層目のセルのｉ型半導体層、第２層目のセルのｎ（またはｐ）型半導体層、第３層目のセルのｎ（またはｐ）型半導体層、とした場合である。

【００６２】この場合、ダイオード素子の不純物ドープ層の層厚を厚くすることができる。

【００６３】図９（太陽電池ｈ）は、ダイオード素子の半導体層を、下から順に、太陽電池素子の第１層目のセルのｉ型半導体層、第２層目のセルのｉ型半導体層、第２層目のセルのｎ（またはｐ）型半導体層、とした場合である。この場合、ダイオード素子の実質的に真性なｉ型半導体層の層厚を厚くすることができる。

【００６４】（ダイオード素子）本発明に係るダイオード素子の実質的に真性な半導体層の層厚としては、約５０ｎｍから約５００ｎｍの範囲が望ましい。約５０ｎｍ未満では半導体層にピンホールを生じ易く、絶縁破壊も生じ易い。また、約５００ｎｍより厚いと該層の内部の電界が弱まり、ダイオード特性の低下を招く。

【００６５】また、本発明に係る、ダイオード素子で実質的に真性な半導体膜と接合される不純物ドープ層の膜厚としては、約５ｎｍ以上であることが望ましい。約５ｎｍ未満では半導体層を均一に形成することが困難で、ダイオード特性の低下を招く。

【００６６】（導電性基板）本発明に係る導電性基板としては、半導体膜形成時に必要とされる温度において変形、歪みが少なく、所望の強度を有し、良好な導電性を有するものであることが好ましい。具体的にはステンレススチール、アルミニウムおよびその合金、鉄およびその合金、銅およびその合金等の金属板、あるいはポリイミド、ポリアミド、ポリエチレンテレフタレート、エポキシ等の耐熱性樹脂やガラス板等の表面に金属単体または合金、および透明導電性酸化物等を蒸着法、スパッタリング法、メッキ法等で導電処理を行ったものが挙げられる。

【００６７】なお、導電性基板には、基板に到達した長波光の反射率の向上、基板材料と半導体層との相互拡散の防止、密着性の向上、基板表面の平滑化等の目的で異種の金属層を半導体層形成側表面に設けても良い。

【００６８】光反射層として設ける場合、このような金属層としてはＡｇ，Ａｌ，Ｃｕ，Ａｕ，ＡｌＳｉ等の可視光から近赤外で反射率が高い金属が適している。

【００６９】また、これらの金属層を設けた場合、これらの金属層と半導体層の間には、金属層から半導体層への金属の拡散を防止するために透明導電層を設けることが望ましい。

【００７０】このような透明導電層としては、ＺｎＯ，SnO_2，In_2O_3，ＩＴＯ等の透明導電性酸化物が最適なものとして挙げられる。

【００７１】（シリコン系非単結晶半導体層の製造装置および製造方法）本発明に係る太陽電池において、シリコン系非単結晶半導体層を形成するにあたっては、各種の製造方法、製造装置を用いることが可能である。

【００７２】図１に示した太陽電池は、例えば、図１０に示した構成の製造装置を用いて作製することができる。図１０に示す製造装置は、プラズマＣＶＤ法による所謂ロール・ツー・ロール方式の連続製造装置である。図１０において、図１０（Ａ）は装置の横方向からみた断面図、図１０（Ｂ）は同装置の上方からみた断面図である。

【００７３】図１０において、１００４Ａ，１００５Ａ，１００６Ａ，１００４Ｂ，１００５Ｂ，１００６ＢはプラズマCVD法によるｎ，ｉ，ｐ（またはｐ，ｉ，ｎ）型層の成膜室、１００１，１００２は帯状の導電性基板の巻き出し室、巻き取り室である。各成膜室の真空チャンバーには放電室１００８が設けられ、放電室内部にグロー放電を生起することによってシリコン系非単結晶半導体膜の堆積が行われる。各成膜室の真空チャンバーは、狭い隙間にＨｅ等のパージガスを流して成膜室間のガスの相互混入を防ぐガスゲート１００７によって接続される。１００３はたとえば厚さ０．１３ｍｍ、幅３６ｃｍのステンレスシートのような帯状の導電性基板であり、供給室１００１から巻き出され、連続的に搬送されながら６つの成膜室１００４Ａ，１００５Ａ，１００６Ａ，１００４Ｂ，１００５Ｂ，１００６Ｂを通過して、巻き取り室１００２に巻き取られる間、その表面に図１０（Ｂ）の導電性基板向こう側の領域に２層のｎｉｐ（またはｐｉｎ）構造の太陽電池素子用のシリコン系非単結晶半導体の積層膜が、図１０（Ｂ）の導電性基板手前側の領域にｉｎ（またはｉｐ）構造のダイオード素子用のシリコン系非単結晶半導体の積層膜が形成され

る。

【0074】なお、図には示していないが、各成膜室には基板を半導体の堆積に適した所定の温度に制御する加熱ヒーター等の温度制御手段、ガス供給手段から各成膜室内に半導体形成用の原料ガスを導入する原料ガス導入手段、排気手段により成膜室を排気し所定の圧力に調整する不図示の排気管、不図示の高周波電源から成膜室内のガスに高周波電力を供給する不図示の放電手段が設けられ、成膜室1004A，1005A，1006A，1004B，1005B，1006Bでは、各放電室1008においてそれぞれ、n，i，p，n，i，p（またはp，i，n，p，i，n）型のシリコン系非単結晶半導体層がプラズマCVD法によって堆積される。

【0075】放電室1008上部には導電性基板1003との間にマスク1009が設けられ、帯状の導電性基板1003上の所定の位置に所望の半導体層が堆積される。

【0076】各放電室1008のどの位置にマスク1009の開口部があり、どの位置で半導体層が堆積されるかを図10（B）に示す。マスク1009の開口部は、同図導電性基板1003の向こう側の太陽電池素子用半導体層形成領域1010と、手前側のダイオード素子用半導体膜形成領域1011とに分離され、同図導電性基板1003の向こう側にnipnip（またはpinpin）構造の太陽電池素子用の半導体積層膜が、手前側にin（またはip）構造のダイオード素子用の半導体積層膜が堆積される。

【0077】このような装置を用いれば、本発明の太陽電池の半導体層を形成することができる。その後、公知の真空蒸着法あるいはスパッタリング法等によりITO，SnO_2等の透明導電膜を形成し、さらに真空蒸着法、スクリーン印刷法等によりAg，Al等の集電電極を形成し、太陽電池素子とダイオード素子の集電電極を導線で接続し、ダイオード素子上に黒色の遮光塗料等を塗布することによって図1に示すような本発明の太陽電池を製造することができる。

【0078】（太陽電池モジュール）本発明に係る太陽電池モジュールとは、上述した太陽電池素子にバイパスダイオード素子を接続した太陽電池を、複数個直列接続し、モジュール化したものを指す。

【0079】バイパスダイオードが無い場合、直列接続されたn個の太陽電池の中で1つの太陽電池が影になると、影になった太陽電池には最大、他の太陽電池素子の開放電圧の（n－1）倍の逆方向電圧が印加されるため、部分的な影ができた時に太陽電池素子にかかる逆方向電圧が太陽電池素子の耐圧を超えない範囲内でしか直列接続数を増やすことができない。

【0080】しかし、本発明の太陽電池は各太陽電池素子毎にバイパスダイオードが接続されているため、モジュール化される際の太陽電池の直列接続数は、所望の出力電圧が得られる様に自由に設定することができる。

【0081】また、本発明において、シリコン系非単結晶半導体からなるバイパスダイオード素子に単結晶半導体からなるダイオードをさらに並列接続してもよいが、太陽電池を直列接続してモジュール化する場合、単結晶半導体からなるダイオードは必ずしも各太陽電池ごとに接続する必要はなく、直列接続された複数の太陽電池に1個の割合で並列接続する様にしてもよい。

【0082】さらに、複数の太陽電池モジュールを直列接続するような場合には、1枚の太陽電池モジュールに単結晶半導体からなるダイオードを1個だけ入れるようにしてもよい。

【0083】

【実施例】以下では、本発明の太陽電池および太陽電池モジュールに関して詳述するが、本発明はこれらの実施例によって何ら限定されるものではない。

【0084】（実施例1）本例では、図10に示した構成の製造装置を用い、導電性基板上にシリコン系非単結晶半導体からなるnipnip構造の太陽電池素子と、シリコン系非単結晶半導体からなるin構造のダイオード素子の半導体膜を連続的に形成し、図1に示した構成の太陽電池を作製した。

【0085】以下では、その作製方法を手順に従って説明する。

（1）SUS430BA製の帯状のステンレス板（幅356mm×長さ200m×厚さ0．13mm）の表面に公知のDCマグネトロンスパッタリング法により裏面反射層として500nmのAg層と、Agの拡散防止層として1000nmのZnO透明導電層とを形成、積層した帯状の導電性基板1003をコイル状に巻いた状態で基板巻き出し室1001にセットした。次に、該導電性基板1003を各ガスゲート1007を介して成膜室1004A，1005A，1006A，1004B，1005B，1006Bを貫通させ、基板巻き取り室1003まで渡し、弛まない程度に張力をかけた。

【0086】なお、基板巻き取り室1003には十分乾燥したアラミド紙製の保護フィルム（幅356mm×長さ200m×厚さ0．05mm）の巻きつけられた不図示のボビンをセットし、表面に半導体層の形成された導電性基板1003とともに該保護フィルムが巻き込まれるようにした。

【0087】（2）導電性基板をセットした後、各成膜室1004A～1006B内を不図示の真空排気ポンプで一度真空排気し、引き続き排気しながらHeガスを導入して約200PaのHe雰囲気中で各成膜室内部を約350℃に加熱ベーキングした。

【0088】（3）加熱ベーキングの後、各室1004A～1006Bをそれぞれ真空排気ポンプで排気しながら、各ガスゲートにゲートガスとしてH_2を各1000sccm，各成膜室の放電室1008にそれぞれの原料

ガスを所定流量導入した。そして、各成膜室を排気する真空排気ポンプと各成膜室の間の排気管に設けた不図示のスロットルバルブの開度を調整することにより、基板巻き出し室1001と基板巻き取り室1002の内部を130Paに、各成膜室1004A～1006Bの各放電室内部を135Paに圧力設定した。

【0089】（4）各室の圧力が安定したところで、基板巻き取り室1002の導電性基板1003の巻き取りボビンを回転させ、導電性基板1003を成膜室1004Aから成膜室1006Bに向かう方向に250mm／minの速度で移動させた。また、各放電室1008に設けた不図示の温度制御手段により、移動する導電性基板が各放電室で所定の温度になるよう温度制御を行った。

【0090】（5）基板の温度が安定したところで、成膜室1004A～1006Bの各放電室に設けた不図示の放電電極に、不図示の高周波電源からマッチング装置を介して高周波電力を投入し、各放電室内の原料ガスをグロー放電分解し、プラズマを発生させた。表1に示した成膜条件により、各成膜室内で連続的に移動する導電性基板上に半導体膜の堆積が行われ、幅356mmの導電性基板上に6mmの間隔をあけて、幅300mmのnipnip構造の2層タンデム型太陽電池素子と幅50mmのin構造のダイオード素子を形成した。

【0091】（6）帯状基板の約170mにわたって半導体膜を堆積形成した後、放電電力の投入と、原料ガスの導入と、導電性基板と成膜室の加熱を停止し、成膜室内のパージを行い、導電性基板および装置内部を十分冷却してから装置を開け、表面に半導体層を形成されコイル状に巻かれた導電性基板を装置から取り出した。

【0092】（7）形成した半導体膜上に、スパッタリング法によって透明導電膜として膜厚70nmのITO導膜を形成し、Agペーストを使ったスクリーン印刷法により集電電極として一定間隔に細線状のAg電極を形成した。なお、透明導電膜と集電電極は半導体膜上にのみ形成し、太陽電池素子上の集電電極とダイオード素子上の集電電極は薄い銅板の導線で接続した。

【0093】（8）ダイオード素子の部分に遮光用の黒色塗料を塗布した後、太陽電池を形成した導電性基板を長さ100mm毎に切断し、幅356mm、長さ100mmの太陽電池を150個作製した。図1は、作製した太陽電池の層構成を示す模式的断面図である。

【0094】（9）この太陽電池を、厚さ0.1mmのフッ素系表面保護シート〔4フッ化エチレンとエチレンの共重合体ETFE（デュポン製テフゼル）〕と厚さ0.3mmの亜鉛塗装鋼板の間に厚さ約0.5mmのEVA耐脂（エチレンビニルアセテート）を介して挟み込み、公知の真空貼り合わせ装置を用いて加熱圧縮することによって樹脂で封止した。

【0095】（10）上記工程（1）～（9）にて作製した太陽電池の電流－電圧特性を調べたところ、ダイオード素子がバイパスダイオードとして動作しており、光が遮断された状態でも、逆方向電圧0.3Vにおいて太陽電池素子のAM1.5（1000W/m²）照射時の短絡電流と同じだけの電流が流れ、暗状態で逆方向に電圧を印加しても太陽電池素子には極めて低い逆方向電圧しか印加されないことが確認された。

【0096】（11）作製した太陽電池に対して光を完全に遮断し、逆方向に1Vの定電圧電源を接続して、湿度95%、温度50℃の環境試験装置に入れ、高温下で部分的な遮光が行われ、逆方向電圧が印加された状態を再現した耐久試験を連続1時間行った。なお、定電圧電源には電流制限回路を設け、太陽電池素子のAM1.5（1000W/m²）照射時の短絡電流以上の電流が流れる場合には、太陽電池素子のAM1.5（1000W/m²）照射時の短絡電流の定電流電源として動作するようにした。

【0097】その結果、耐久試験前後で、湿度50%、温度25℃、暗状態における太陽電池の並列抵抗は、試験前の平均値が10MΩcm²、試験後の平均値が100kΩcm²と低下がみられたものの実用上何等問題のない水準に保たれており、太陽電池素子の曲線因子、開放電圧には殆ど変化のないことが分かった。

【0098】また、耐久試験後の太陽電池の湿度50%、温度25℃でのAM1.5（1000W/m²）照射時の光電変換効率は試験前の平均95%の値で殆ど変化していなかった。

【0099】（比較例1）本例では、図10の装置を用い太陽電池を作製する際に、各放電室のマスクのダイオード素子用開口部1011を塞ぎ、ダイオード素子用の半導体膜を堆積しないようにした点が実施例1と異なる。

【0100】本例の太陽電池は、図1の太陽電池素子101の部分からなり、ダイオード素子をもたない。したがって、実施例1に記載した、遮光塗料110の塗布や導線109の結線は行わなかった。

【0101】このようにして作製した太陽電池を実施例1と同条件で樹脂で封止し、実施例1と同条件で、高温下で部分的な遮光が行われ、逆方向電圧が印加された状態を再現した耐久試験を連続1時間行った。

【0102】その結果、耐久試験前後で、湿度50%、温度25℃、暗状態での太陽電池の並列抵抗は、試験前の平均値が10MΩcm²、試験後の平均値が1kΩcm²と大きく低下しており、太陽電池素子の電流－電圧曲線に影響が現われ、曲線因子、開放電圧が大きく低下した。

【0103】また、耐久試験後の太陽電池の湿度50%、温度25℃でのAM1.5（1000W/m²）照射時の光電変換効率は試験前の平均70%の値まで低下した。

【0104】なお、ダイオード素子を接続しない太陽電池素子の耐久試験前の光電変換効率は、実施例1のダイオード素子を接続した太陽電池の耐久試験前の光電変換効率と全く同じで、実施例1においてダイオード素子の接続によって太陽電池素子の光電変換効率に影響がなかったことが確認された。

【0105】（実施例2）本例では、図10に示した構成の製造装置を用い、成膜室1004A，1006A，1004B，1006Bで成膜する半導体膜の導電型を逆極性として、図1に示した構成の太陽電池を作製した点が実施例1と異なる。

【0106】すなわち、導電性基板上にシリコン系非単結晶半導体からなるｐｉｎｐｉｎ構造の太陽電池素子と、シリコン系非単結晶半導体からなるｉｐ構造のダイオード素子の半導体膜を連続的に形成した。表2は各成膜室における半導体膜の作製条件である。

【0107】このようにして作製した太陽電池を実施例1と同条件で樹脂で封止し、実施例1と同条件で、高湿下で部分的な遮光が行われ、逆方向電圧が印加された状態を再現した耐久試験を連続1時間行った。

【0108】その結果、耐久試験前後で、湿度50%、温度25℃、暗状態での太陽電池の並列抵抗は、試験前の平均値が10MΩcm²、試験後の平均値が100kΩcm²と低下がみられたものの実用上何等問題のない水準に保たれており、太陽電池素子の曲線因子、開放電圧には殆ど変化がなかった。

【0109】また、耐久試験後の太陽電池の湿度50%、温度25℃でのAM1．5（1000W/m²）照射時の光電変換効率は試験前の平均95%の値で殆ど変化していなかった。

【0110】（実施例3）本例では、シリコン系非単結晶半導体からなるｉｎ構造のダイオード素子に、単結晶シリコンからなるダイオードを並列接続して、図4に示した構成の太陽電池を作製した点が実施例1と異なる。

【0111】以下では、その作製方法を手順に従って説明する。

（1）図10に示した構成の製造装置を用い、実施例1と同様にして、導電性基板上にシリコン系非単結晶半導体からなるｎｉｐｎｉｐ構造の太陽電池素子と、シリコン系非単結晶半導体からなるｉｎ構造のダイオード素子の半導体膜を連続的に形成した。

【0112】（2）順方向電流の最大定格が太陽電池素子のAM1．5（1000W/m²）照射時の短絡電流の3倍で、順方向電流が太陽電池素子のAM1．5（1000W/m²）照射時の短絡電流と等しい時の順方向電圧が約0．8Vの単結晶シリコンからなるダイオードを導線を介して並列接続し、図4に示した構成の太陽電池を製造した。

【0113】なお、シリコン系非単結晶半導体からなるダイオード素子と単結晶シリコンからなるダイオードとは、順方向が同じ向きになるようにして並列接続した。

【0114】このようにして作製した太陽電池を実施例1と同条件で樹脂で封止し、実施例1と同条件で、高湿下で部分的な遮光が行われ、逆方向電圧が印加された状態を再現した耐久試験を連続1時間行った。

【0115】その結果、耐久試験前後で、湿度50%、温度25℃、暗状態での太陽電池の並列抵抗は試験前の平均値が5MΩcm²、試験後の平均値が50kΩcm²と低下がみられたものの実用上何等問題のない水準に保たれており、太陽電池素子の曲線因子、開放電圧には殆ど変化がなかった。

【0116】また、耐久試験後の太陽電池の湿度50%、温度25℃でのAM1．5（1000W/m²）照射時の光電変換効率は試験前の平均95%の値で殆ど変化していなかった。

【0117】（実施例4）本例では、図10に示した構成の製造装置を一部変更し、各成膜室1005A，1004Bで放電室1008のマスク1009の開口部を2箇所に分けず、ダイオード素子用半導体膜形成領域1011を太陽電池素子用半導体膜形成領域1010とが連続するようにして、図2に示した構成の太陽電池を作製した点が実施例1と異なる。

【0118】すなわち、導電性基板上にシリコン系非単結晶半導体からなるｎｉｐｎｉｐ構造の太陽電池素子と、シリコン系非単結晶半導体からなるｉｎ構造のダイオード素子の半導体膜を連続的に形成した。

【0119】このようにして作製した太陽電池を実施例1と同条件で樹脂で封止し、実施例1と同条件で、高湿下で部分的な遮光が行われ、逆方向電圧が印加された状態を再現した耐久試験を連続1時間行った。

【0120】その結果、耐久試験前後で、湿度50%、温度25℃、暗状態での太陽電池の並列抵抗は試験前の平均値が1MΩcm²、試験後の平均値が100kΩcm²と低下がみられたものの実用上何等問題のない水準に保たれており、太陽電池素子の曲線因子、開放電圧には殆ど変化がなかった。

【0121】また、耐久試験後の太陽電池の湿度50%、温度25℃でのAM1．5（1000W/m²）照射時の光電変換効率は試験前の平均95%の値で殆ど変化していなかった。

【0122】（実施例5）本例では、図10に示した構成の製造装置を一部変更し、各成膜室1005A，1004Bで、導電性基板の表側に太陽電池素子用の半導体膜が幅350mmで、導電性基板の裏側にダイオード素子用の半導体膜が幅150mmで形成されるようにして、図3に示した構成の太陽電池を作製した点が実施例1と異なる。

【0123】すなわち、導電性基板の表裏にシリコン系非単結晶半導体からなるｎｉｐｎｉｐ構造の太陽電池素子と、シリコン系非単結晶半導体からなるｉｎ構造のダ

イオード素子の半導体膜を連続的に形成した。

【0124】なお、ダイオード素子は導電性基板の裏面に形成され、入射光が遮られるためダイオード素子には遮光塗料の塗布は行わなかった。

【0125】このようにして作製した太陽電池を実施例1と同条件で樹脂で封止し、実施例1と同条件で、高湿下で部分的な遮光が行われ、逆方向電圧が印加された状態を再現した耐久試験を連続1時間行った。

【0126】その結果、耐久試験前後で、湿度50%、温度25℃、暗状態での太陽電池の並列抵抗は試験前の平均値が1MΩcm²、試験後の平均値が100kΩcm²と低下がみられたものの実用上何等問題のない水準に保たれており、太陽電池素子の曲線因子、開放電圧には殆ど変化がなかった。

【0127】また、耐久試験後の太陽電池の湿度50%、温度25℃でのAM1.5（1000W/m²）照射時の光電変換効率は試験前の平均95%の値で殆ど変化していなかった。

【0128】（実施例6）本例では、図10に示した構成の製造装置を一部変更し、成膜室1006Bと基板巻き取り室1002との間に更に3つの成膜室、n（p）型層成膜室1004C、i型層成膜室1005C、p（n）型層成膜室1006Cを追加した。

【0129】これにより、nipnipnip（またはpinpinpin）構造の3層タンデム型太陽電池素子用の半導体膜が形成され、成膜室1005A、1005B、1004Cにおいて導電性基板の一部にダイオード素子用の半導体膜が形成されるようにして、図5に示した構成の太陽電池を作製した点が実施例1と異なる。

【0130】すなわち、各成膜室の成膜条件を表3に示したように変更した以外は実施例1と同様にして、導電性基板上にシリコン系非単結晶半導体からなるnipnipnip構造の太陽電池素子と、シリコン系非単結晶半導体からなるin構造のダイオード素子の半導体膜を連続的に形成した。

【0131】このようにして作製した太陽電池を実施例1と同条件で樹脂で封止し、実施例1と同条件で、高湿下で部分的な遮光が行われ、逆方向電圧が印加された状態を再現した耐久試験を連続1時間行った。

【0132】その結果、耐久試験前後で、湿度50%、温度25℃、暗状態での太陽電池の並列抵抗は試験前の平均値が10MΩcm²、試験後の平均値が100kΩcm²と低下がみられたものの実用上何等問題のない水準に保たれており、太陽電池素子の曲線因子、開放電圧には殆ど変化がなかった。

【0133】また、試験後の太陽電池の湿度50%、温度25℃でのAM1.5（1000W/m²）照射時の光電変換効率は試験前の平均95%の値で殆ど変化していなかった。

【0134】（実施例7）本例では、実施例6で作製した太陽電池素子とダイオード素子から構成された太陽電池を10段直列接続して、太陽電池モジュールを作製した。

【0135】なお、各太陽電池には順方向電流の最大定格が太陽電池素子のAM1.5（1000W/m²）照射時の短絡電流の3倍で、順方向電流が太陽電池素子のAM1.5（1000W/m²）照射時の短絡電流と等しい時の順方向電圧が約0.8Vの単結晶シリコンからなるダイオードを並列に接続した。

【0136】このようにして作製した太陽電池モジュールを実施例1と同条件で樹脂で封止し、10段直列接続した太陽電池の中の1個だけをマスクで完全に遮光し、逆方向に3Vの定電圧電源を接続して湿度95%、温度50℃の環境試験装置に入れ、高湿下で部分的な遮光が行われ、逆方向電圧が印加された状態を再現した耐久試験を連続1時間行った。

【0137】なお、定電圧電源には電流制限回路を設け、太陽電池素子のAM1.5（1000W/m²）照射時の短絡電流以上の電流が流れる場合には、太陽電池素子のAM1.5（1000W/m²）照射時の短絡電流の定電流電源として動作するようにした。

【0138】その結果、耐久試験前後で、光を遮断した太陽電池の湿度50%、温度25℃、暗状態での並列抵抗は試験前の平均値が5MΩcm²、試験後の平均値が50kΩcm²と低下がみられたものの実用上何等問題のない水準に保たれており、太陽電池素子の曲線因子、開放電圧には殆ど変化がなかった。

【0139】また、試験後の遮光マスクを外した太陽電池モジュールの湿度50%、温度25℃でのAM1.5（1000W/m²）照射時の光電変換効率は試験前の平均95%の値で殆ど変化していなかった。

【0140】（比較例2）本例では、実施例6で作製した太陽電池モジュールにおいて、ダイオード素子の集電電極を太陽電池素子に接続する導線を除き、シリコン系非単結晶半導体からなるダイオード素子が接続されない様にして、シリコン系非単結晶半導体からなるin構造のダイオード素子の接続されていない太陽電池モジュールとした点が実施例7と異なる。なお、太陽電池モジュールの10段直列接続された各太陽電池には実施例7と同様に単結晶シリコンからなるダイオードを並列に接続した。

【0141】このようにして作製した太陽電池モジュールを実施例1と同条件で樹脂で封止し、10段直列接続した太陽電池の中の1個だけをマスクで完全に遮光し、逆方向に3Vの定電圧電源を接続して湿度95%、温度50℃の環境試験装置に入れ、高湿下で部分的な遮光が行われ、逆方向電圧が印加された状態を再現した耐久試験を連続1時間行った。

【0142】なお、定電圧電源には電流制限回路を設け、太陽電池素子のAM1.5（1000W/m²）照

射時の短絡電流以上の電流が流れる場合には、太陽電池素子のAM1．5（1000W／m²）照射時の短絡電流の定電流電源として動作するようにした。

【0143】その結果、耐久試験前後で、光を遮断した太陽電池の湿度50％、温度25℃、暗状態での並列抵抗は試験前の平均値が5MΩcm²、試験後の平均値が1kΩcm²と大きく低下しており、太陽電池素子の電流－電圧曲線に影響が現われ、曲線因子、開放電圧が大

きく低下した。

【0144】また、試験後の太陽電池モジュールの湿度50％、温度25℃でのAM1．5（1000W／m²）照射時の光電変換効率は試験前の平均70％の値まで低下した。

【0145】

【表1】

21

成膜室		1004A	1005A	1006A
太陽電池素子用堆積膜		n型a-Si 40nm	i型a-SiGe 100nm	p型微結晶Si 10nm
ダイオード素子用堆積膜			i型a-SiGe 100nm	
放電室搬送方向長さ(cm)		25	50	25
原料ガス流量 (sccm)	SiH_4	15	140	3
	GeH_4		60	
	H_2	150	500	500
	PH_3	1		
	BF_3			0.5
圧力 (Pa)		135	135	135
放電電力 (W)		50	200	500
基板加熱温度 (℃)		300	300	200
成膜室		1004B	1005B	1006B
太陽電池素子用堆積膜		n型a-Si 20nm	i型a-Si 100nm	p型微結晶Si 10nm
ダイオード素子用堆積膜		n型a-Si 20nm		
放電室搬送方向長さ(cm)		25	50	25
原料ガス流量 (sccm)	SiH_4	10	200	3
	GeH_4			
	H_2	150	500	500
	PH_3	1		

23				24
	BF_3			0.1
圧力	(Pa)	135	135	135
放電電力	(W)	50	200	500
基板加熱温度	(℃)	300	200	200

【0146】　　＊　＊【表2】

25

成膜室		1004A	1005A	1006A
太陽電池素子用堆積膜		p型a-Si 40nm	i型a-SiGe 100nm	n型微結晶Si 10nm
ダイオード素子用堆積膜			i型a-SiGe 100nm	
放電室搬送方向長さ(cm)		25	50	25
原料ガス流量 (sccm)	SiH_4	15	140	3
	GeH_4		60	
	H_2	150	500	500
	PH_3			0.5
	BF_3	1		
圧力 (Pa)		135	135	135
放電電力 (W)		50	200	500
基板加熱温度 (℃)		300	300	200
成膜室		1004B	1005B	1006B
太陽電池素子用堆積膜		p型a-Si 20nm	i型a-Si 100nm	n型微結晶Si 10nm
ダイオード素子用堆積膜		p型a-Si 20nm		
放電室搬送方向長さ(cm)		25	50	25
原料ガス流量 (sccm)	SiH_4	10	200	3
	GeH_4			
	H_2	150	500	500
	PH_3			0.1

27　　28

	BF₃	1		
圧力	(Pa)	135	135	135
放電電力	(W)	50	200	500
基板加熱温度	(℃)	300	200	200

【0147】　　＊　＊【表3】

29

成膜室		1004A	1005A	1006A
太陽電池素子用堆積膜		n型a-Si 40nm	i型a-SiGe 100nm	p型微結晶Si 10nm
ダイオード素子用堆積膜			i型a-SiGe 100nm	
放電室搬送方向長さ(cm)		25	50	25
原料ガス流量 (sccm)	SiH_4	15	140	3
	GeH_4		60	
	H_2	150	500	500
	PH_3	1		
	BF_3			0.5
圧力 (Pa)		135	135	135
放電電力 (W)		50	200	500
基板加熱温度 (℃)		300	300	200
成膜室		1004B	1005B	1006B
太陽電池素子用堆積膜		n型a-Si 20nm	i型a-SiGe 100nm	p型微結晶Si 10nm
ダイオード素子用堆積膜			i型a-SiGe 100nm	
放電室搬送方向長さ(cm)		25	50	25
原料ガス流量 (sccm)	SiH_4	10	160	3
	GeH_4		40	
	H_2	150	500	500
	PH_3	1		

31				32
	BF_3			0.5
圧力 (Pa)		135	135	135
放電電力 (W)		50	200	500
基板加熱温度 (℃)		250	250	200
成膜室		1004C	1005C	1006C
太陽電池素子用堆積膜		n型a－Si 20nm	i型a－Si 100nm	p型微結晶Si 10nm
ダイオード素子用堆積膜		n型a－Si 20nm		
放電室搬送方向長さ(cm)		25	50	25
原料ガス流量 (sccm)	SiH_4	10	200	3
	GeH_4			
	H_2	150	500	500
	PH_3	1		
	BF_3			0.1
圧力 (Pa)		135	135	135
放電電力 (W)		50	200	500
基板加熱温度 (℃)		200	200	200

【0148】

【発明の効果】以上説明したように、本発明によれば、太陽電池モジュールに部分的な影が生じても各太陽電池に印加される逆方向電圧が極めて低いため、裏面反射層や集電電極にAg等の金属を用いても高湿度下での部分的な光遮断による太陽電池モジュールの短絡の発生が抑制され、太陽電池の性能を低下させることなく、太陽電池および太陽電池モジュールの信頼性を格段に高めることができる太陽電池が得られる。

【0149】また、本発明によれば、同一の導電性基板上にその表面を絶縁処理することなく、太陽電池素子とバイパスダイオード素子を同時に形成することができ、生産性に優れたバイパスダイオード付きの太陽電池および太陽電池モジュールを提供することができる。

【図面の簡単な説明】

【図1】本発明に係る太陽電池の一例を示す模式的断面＊図である。

【図2】本発明に係る太陽電池の他の一例を示す模式的断面図である。

【図3】本発明に係る太陽電池の他の一例を示す模式的断面図である。

【図4】本発明に係る太陽電池の他の一例を示す模式的断面図である。

【図5】本発明に係る太陽電池の他の一例を示す模式的断面図である。

【図6】本発明に係る太陽電池の他の一例を示す模式的断面図である。

【図7】本発明に係る太陽電池の他の一例を示す模式的断面図である。

【図8】本発明に係る太陽電池の他の一例を示す模式的断面図である。

【図9】本発明に係る太陽電池の他の一例を示す模式的

断面図である。

【図10】本発明に係る太陽電池の作製に用いた製造装置の一例を示す模式的断面図である。

【符号の説明】

101、201、301、401、501、601、701、801、901太陽電池素子、

102、202、302、402、502、602、702、802、902ダイオード素子、

103、203、303、403、503、603、703、803、903、1003　導電性基板、

104A、204A、304A、404A、504A、604A、704A、804A、904A、104B、204B、304B、404B、504B、604B、704B、804B、904B、504C、604C、704C、804C、904C、104D、304D、404D、504D　n（またはp）型半導体層、

105A、205A、305A、405A、505A、605A、705A、805A、905A、105B、205B、305B、405B、505B、605B、705B、805B、905B、505C、605C、705C、805C、905C、105D、305D、405D、505D　実質的に真性な半導体層、

106A、206A、306A、406A、506A、606A、706A、806A、906A、106B、206B、306B、406B、506B、606B、706B、806B、906B、506C、606C、706C、806C、906C　p（またはn）型半導体層、

107、207、307、407、507、607、707、807、907、107D、207D、307D、407D、507D、607D、707D、807D、907D　透明導電膜、

108、208、308、408、508、608、708、808、908、108D、208D、308D、408D、508D、608D、708D、808D、908D　集電電極、

109、209、309、409、509、609、709、809、909導線、

110、210、410、510、610、710、810、910　遮光塗料、

411　単結晶半導体からなるダイオード、

1001　基板巻き出し室、

1002　基板巻き取り室、

1004A、1004B　n（またはp）型半導体層成膜室、

1005A、1005B　実質的に真性な半導体層の成膜室、

1006A、1006B　p（またはn）型半導体層成膜室、

1007　ガスゲート、

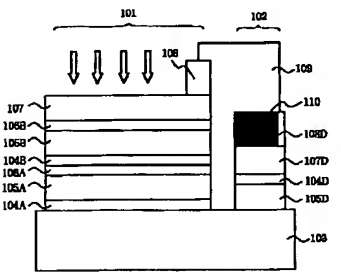
1008　放電室、

1009　マスク、

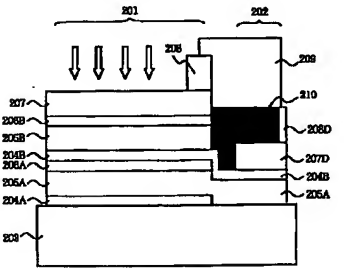
1010　太陽電池素子用半導体膜形成領域、

1011　ダイオード素子用半導体膜形成領域。

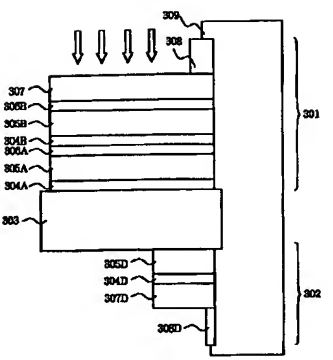
【図1】



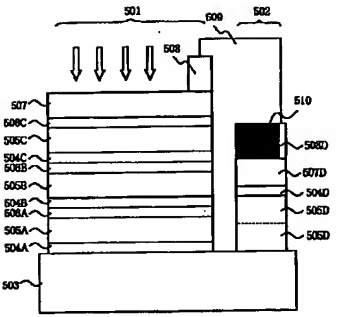
【図2】



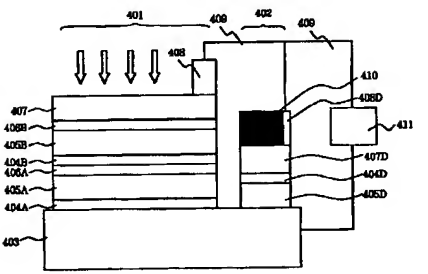
【図3】


309
308
307
306B
305B
304B
306A
305A
304A
303
301
305D
304D
307D
306D
302

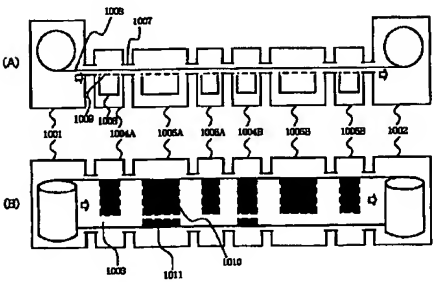
【図5】


501
509
502
508
507
506C
505C
504C
506B
505B
504B
506A
505A
504A
503
510
508D
507D
504D
506D
505D

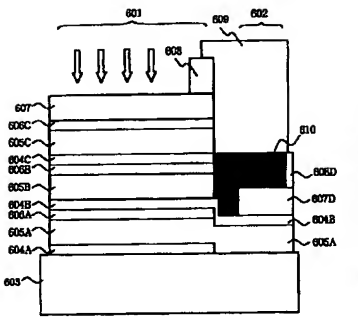
【図4】


401
409
402
409
408
410
406D
411
407
406B
405B
404B
406A
405A
404A
403
407D
404D
405D

【図10】


1008
1007
(A)
1009
1006
1001
1004A
1005A
1006A
1004B
1005B
1006B
1002
(B)
1003
1011
1010

【図6】


601
609
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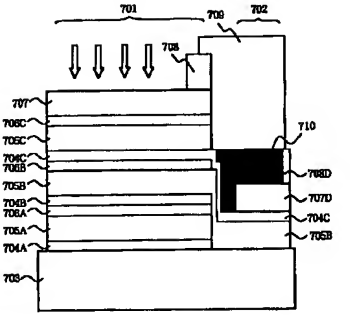
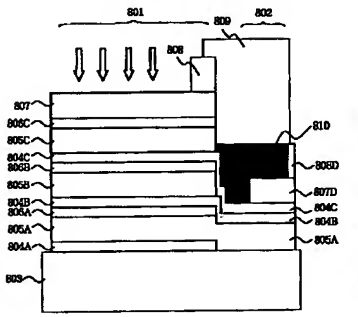
607
606C
605C
604C
606B
605B
604B
606A
605A
604A
603
610
606D
607D
604B
605A

【図7】


701
709
702
708
707
706C
705C
706C
706B
705B
704B
706A
705A
704A
703
710
706D
707D
704C
705B

【図8】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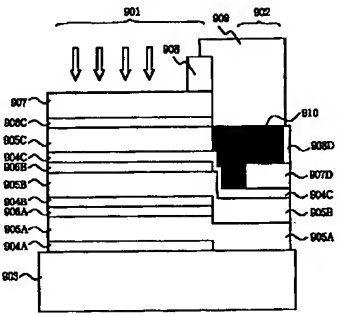
【図9】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* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The tandem-die solar battery element which carried out two or more laminatings of nip or the pin junction which consists a n-type semiconductor of a silicon system non-single crystal semiconductor on a conductive substrate when n and an i-type semiconductor are set to i and a p type semiconductor is set to p, In the solar battery which serves as said solar battery element from the by-pass diode by which parallel connection was carried out to said solar battery element so that it may become hard flow electrically The solar battery characterized by being in which said by-pass diode becomes from the silicon system non-single crystal semiconductor by which deposition formation was carried out on said conductive substrate, or the diode component of ip junction.
[Claim 2] i in said diode component is a solar battery according to claim 1 characterized by consisting of amorphous silicon germanium.
[Claim 3] The solar battery according to claim 1 or 2 which ****** having the diode which turns into said by-pass diode from the single crystal semiconductor by which parallel connection was carried out to said by-pass diode so that it may become the forward direction electrically.
[Claim 4] The solar cell module which ****** having carried out the series connection of two or more solar batteries of a publication to claim 1 thru/or at least 1 term of 3.

[Translation done.]

* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to a solar battery and a solar cell module. More, it is related with the solar battery and solar cell module which formed the by-pass diode by which parallel connection was carried out to the solar battery element so that it may become hard flow electrically [a solar battery element] in a detail.
[0002]
[Description of the Prior Art] The modularization of current and the solar battery for power is carried out in the form of the component array which generally carried out the series connection of two or more **** cell components.
[0003] The sum total of the generated voltage of the component which has generated others is impressed to the component which became a shadow when operating by the series connection and some components of a component array went into the shadow in the form of reverse voltage, and when it becomes the value to which this reverse voltage exceeds pressure-proofing of a component, there is a problem that destruction of a component arises.
[0004] As an approach of preventing destruction of the component by such partial optical cutoff, the approach of connecting the so-called by-pass diode to juxtaposition is learned by the reverse sense, and, generally it is carried out to each component by which the series connection was carried out. Moreover, forming a by-pass diode in a photovoltaic cell and coincidence is also performed, and some techniques which form a by-pass diode on the same substrate are proposed also in the solar battery using a non-single crystal semiconductor.
[0005] With the solar battery using the amorphous silicon deposited on the insulating substrate, a part of component is separated, electrode connection is made at the reverse sense and the technique which forms a by-pass diode is indicated by JP,63-13358,B. The technique which carries out separation formation of an amorphous silicon solar cell and the Schottky barrier diode on the same substrate is indicated by JP,2-5575,B.
[0006] Thus, if parallel connection of the by-pass diode is carried out to each solar battery element, when some components of a component array become a shadow, for the component which became a shadow, the reverse voltage more than the forward voltage of a by-pass diode is not impressed, but can prevent destruction of the solar battery element by high-tension impression.
[0007] However, even if it has connected the by-pass diode in this way, under certain conditions, the solar battery element which became a shadow selectively can be in a short circuit condition.
[0008] That is, reverse voltage of this level is impressed to the solar battery element by which optical cutoff of the forward voltage of a by-pass diode was selectively carried out about abbreviation 0.8V in the case of the pn junction diode of single crystal silicon. Usually, although a short circuit is not produced in an amorphous silicon solar battery element on an electrical potential difference of this level When the metal which ionizes as the electrode and rear-face reflective film of a solar battery element, and is easy to move is used, In the condition that moisture invaded into the semi-conductor film of a solar battery element through the membranous edge, a crack, a pinhole, etc., in order for a metal ion to move in the inside of the semi-conductor film, to form a partial track in the semi-conductor film and to generate a short circuit cable run also on an electrical potential difference of this level, there is a problem that a dangerous condition arises.
[0009] Below, the layer of Ag with a reflection factor high as a light reflex layer on the back is formed on a conductive substrate, the laminating of n of amorphous Si, i, and the p type semiconductor layer is carried out to this order on it, the case of the solar battery element which formed the transparent electrode on it further is taken up, and the above-mentioned problem is explained more concretely.
[0010] The nip junction structure which arranges a p type semiconductor layer to an optical incidence side in the solar battery using a non-single-crystal-silicon system semi-conductor is in use, in order to use incident light effectively and to make the amount of generating currents increase, it is also performed that the rear-face light reflex layer in which the

light which penetrated the semi-conductor layer once is reflected with the rear face forms [many], and this example is the configuration of a very general solar battery element.

[0011] Even if moisture invades into a semi-conductor layer and a part of Ag of a light reflex layer cation-izes by such solar battery element since a conductive substrate side generates a negative electrical potential difference where an optical exposure is usually made the whole surface at the time of a generation of electrical energy, Ag ion does not move in the inside of the semi-conductor film.

[0012] however, after moisture has invaded into the semi-conductor film with such a solar battery, when optical cutoff of this solar battery element is selectively carried out in a component array If a negative electrical potential difference is impressed to a transparent electrode side, a part of Ag of a light reflex layer cation-izes, forward Ag ion moves toward the transparent electrode with which the inside of the semi-conductor film was impressed to the negative electrical potential difference, and it is possible to deposit as Ag again by the transparent electrode side. The danger that the short circuit cable run of partial Ag will be formed into the semi-conductor film by this is high.

[0013] Although it is thought that it generates and the phenomenon of ionization of such a metal ion, migration, and a deposit advances in proportion [almost] to the electrical potential difference impressed also with the forward voltage of about 0.8 V of the pn junction diode of single crystal silicon, if this phenomenon advances more than fixed, a short circuit cable run will be formed in the semi-conductor film, and it is thought that a short-circuit current increases rapidly.

[0014] Such a phenomenon is avoidable if trespass of the moisture of not using a metal which is ionized at the semi-conductor film rear face, or a steam can be prevented thoroughly.

[0015] However, it is necessary to use the metal of high conductivity and a high reflection factor as a current collection electrode or a rear-face reflecting layer, and easy to tend ionize metals used as such a metal, such as silver and copper. [many]

[0016] Moreover, when using it by the outdoor severe environmental condition over many years as a solar battery for power, if it is very difficult for a module to guarantee perfect water proof and the cure against water proof of closing the whole solar battery element with glass thoroughly is performed, modular weight will become very heavy and the installation approach will be limited. Moreover, the problem that cost starts obtaining generating cost equivalent to commercial power as an object for power too much is also produced.

[0017] The solar battery using amorphous silicon indicated by aforementioned JP,63-13358,B is deposited on an insulating substrate. By the approach of separating a part of component, and making electrode connection and forming a by-pass diode in the reverse sense The forward voltage of the photovoltaic cell which consists of a pin junction of amorphous silicon is about 1.0V. Even if it is equivalent to the forward voltage of the diode which consists of pn junction of single crystal silicon and changes and adopts it as single crystal silicon diode, there is no effectiveness in controlling generating of a short circuit of the semi-conductor film by the above-mentioned partial light cutoff under highly humid. In the case of the tandem-die structure to which the solar battery element carried out the laminating of two or more nip junction especially, since the open circuit voltage of a solar battery element is high, there is a problem that the forward voltage of a by-pass diode becomes quite high in proportion to the open circuit voltage of a solar battery element.

[0018] On the other hand, by the approach of forming an amorphous silicon solar cell and a Schottky barrier diode on the same substrate indicated by aforementioned JP,2-5575,B, it is thought that effectiveness is in control of the short circuit by the partial light cutoff under highly humid if it is changed and adopted as the pn junction diode of single crystal silicon since the forward voltage of a Schottky barrier diode is lower than the forward voltage of pn junction diode.

[0019] however, by the approach indicated by aforementioned JP,2-5575,B When a solar battery element and diode are formed on the same conductive substrate, unless it prepares an insulating layer and the electrode of a solar battery element and diode is thoroughly separated on a conductive substrate Since a solar battery element and diode become the polarity of this direction to a conductive substrate, Parallel connection of the diode could not be carried out to a solar battery element to hard flow, but there was a problem that it could not be used as a by-pass diode of what can be used as blocking diodes of an antisuckback.

[0020]

[Problem(s) to be Solved by the Invention] This invention controls generating of a short circuit of the solar cell module by the partial optical cutoff under high humidity, and aims at offering a reliable solar battery and a reliable solar cell module.

[0021]

[Means for Solving the Problem] The tandem-die solar battery element which carried out two or more laminatings of nip or the pin junction to which the solar battery of this invention consists of a silicon system non-single crystal

semiconductor on a conductive substrate when n and an i-type semiconductor are set to i and it sets a p type semiconductor to p for a n-type semiconductor, In the solar battery which serves as said solar battery element from the by-pass diode by which parallel connection was carried out to said solar battery element so that it may become hard flow electrically It is characterized by being in which said by-pass diode becomes from the silicon system non-single crystal semiconductor by which deposition formation was carried out on said conductive substrate, or the diode component of ip junction.

[0022] Moreover, as for i in said diode component, consisting of amorphous silicon germanium is desirable.

[0023] Furthermore, as for said by-pass diode, it is desirable to have the diode which consists of a single crystal semiconductor by which parallel connection was carried out to said by-pass diode so that it may become the forward direction electrically.

[0024] The solar cell module of this invention ****** having carried out the series connection of two or more solar batteries mentioned above.

[0025]

[Function] The tandem-die solar battery element which carried out two or more laminatings of nip or the pin junction which consists a n-type semiconductor of a silicon system non-single crystal semiconductor on a conductive substrate when n and an i-type semiconductor are set to i and a p type semiconductor is set to p in invention concerning claim 1, In the solar battery which serves as said solar battery element from the by-pass diode by which parallel connection was carried out to said solar battery.element so that it may become hard flow electrically Since it is in which said by-pass diode becomes from the silicon system non-single crystal semiconductor by which deposition formation was carried out on said conductive substrate, or the diode component of ip junction, An insulating layer can be prepared on said conductive substrate, it is not necessary to separate thoroughly the electrode of said solar battery element and said by-pass diode and, and forward voltage of a diode component can be carried out to 0.45-0.5V of abbreviation one half as compared with the diode component of pin or nip junction.

[0026] Although forward voltage becomes still lower and it is based also on the presentation ratio of Si and germanium in invention concerning claim 2 when i in said diode component is written as amorphous silicon germanium and narrow a-SiGe of a band gap is used for an i-type semiconductor layer, it can lower to about 0.3v.

[0027] In invention concerning claim 3, since it has the diode which consists of a single crystal semiconductor by which parallel connection was carried out to said by-pass diode, reduction in the forward voltage of a by-pass diode and coexistence of buildup of allowable-current capacity can be aimed at, so that it may become the forward direction electrically [said by-pass diode].

[0028] Reduction of the forward voltage by claims 1-3 mentioned above brings about the further lowering of the reverse voltage impressed to a protection-from-light component, even if partial optical cutoff arises in the array of a tandem-die solar battery element.

[0029] consequently, dielectric breakdown of the component by high tension -- from the first -- half a solar battery element -- thin -- a body membrane -- when moisture invades, the solar battery which can be substantially controlled by the short circuit of the component by migration of a metal ion is obtained.

[0030] In invention concerning claim 4, since the series connection of two or more solar batteries of a publication was carried out to at least 1 term of claims 1-3, generating of a short circuit of the solar cell module by the partial optical cutoff under high humidity is controlled. Consequently, a reliable solar cell module is obtained.

[0031]

[Embodiment of the Invention]

(Solar battery) Fundamentally, the solar battery concerning this invention consists of a conductive substrate, a tandem-die solar battery element which consists of two or more nip (or pin) junction, and a diode component which consists of in (or ip) junction. Actually, many solar batteries shown below can be considered from the arrangement relation of the number which nip (or pin) junction piles up, and a solar battery element and a diode component.

[0032] Below, the solar battery concerning this invention is explained to a detail, referring to a drawing.

((a) Solar battery) Drawing 1 is the typical sectional view showing an example of the solar battery concerning this invention, and calls a solar battery a henceforth. A solar battery a is the case where a solar battery element and a diode component are on the same side of a conductive substrate, and the solar battery element and the diode component are electrically connected with the conductive substrate through lead wire.

[0033] drawing 1 -- setting -- a solar battery element 101 -- the conductive substrate 103 top -- n (or p) mold semi-conductor layer 104A -- substantial -- genuineness semi-conductor layer 105A, p (or n) mold semi-conductor layer 106A, and n (or p) mold semi-conductor layer 104B -- it consists of intrinsic semi-conductor layer 105B, p (or n) mold semi-conductor layer 106B, a transparent electrode 107, and a current collection electrode 108 substantially.

[0034] Moreover, the diode component 102 is formed on the same conductive substrate 103 as a solar battery element,

and consists of intrinsic semi-conductor layer 105D, n (or p) mold semi-conductor layer 104D, transparent electrode 107D, and current collection electrode 108D substantially.

[0035] By the optical incidence from a transparent electrode side, the electromotive force of the sense forward (or negative) in the up current collection electrode 108 side occurs [the conductive substrate 103 side] in negative (or forward) in a solar battery element 101.

[0036] On the other hand, it is shaded by the diode component 102 by the protection-from-light coating 110 grade, optical incidence to a semi-conductor layer is not performed, and photoelectromotive force is not generated. By connecting the current collection electrode 108 of a solar battery element 101, and current collection electrode 108D of a diode component with lead wire 109 from the conductive substrate 103, since the sense of current collection electrode 108D HE is the forward direction (or hard flow), parallel connection of the diode component 102 is carried out to a solar battery element 101 to hard flow, and the diode component 102 acts as a by-pass diode.

[0037] In this invention, since a solar battery element has the structure of a tandem die, it generates a high electrical potential difference. When an amorphous silicon system ingredient is used as a semi-conductor layer, i type layer occurs with the nipnip two-layer tandem-die component of a-Si/a-Si, and the high open circuit voltage of about 2.6 V occurs with about 1.8V and the three layer tandem-die component of nipnipnip(s) of a-Si/a-Si/a-SiGe.

[0038] However, since the by-pass diode component of this invention is independent in or ip junction structure, the forward voltage becomes abbreviation half [of the forward voltage of independent pin or nip junction diode]. The forward voltage of the by-pass diode component of this invention is lower than the forward voltage of the diode which consists of pn junction of single crystal silicon, and when an i-type semiconductor layer is a-Si, it becomes Abbreviation 0.45-0.5V. Moreover, when narrow a-SiGe of a band gap is used for an i-type semiconductor layer, forward voltage becomes still lower, and although based also on the presentation ratio of Si and germanium, it can be lowered to about 0.3v.

[0039] dielectric breakdown of the component according [for this low forward voltage, even if partial optical cutoff arises in the array of a tandem-die solar battery element, the reverse voltage impressed to a protection-from-light component becomes very low, and] to high tension -- from the first -- half a solar battery element -- thin -- a body membrane -- when moisture invades, the short circuit of the component by migration of a metal ion is controlled substantially.

[0040] In this invention, it is desirable to carry out the laminating of the transparent electrodes, such as ITO (In_2O_3+SnO_2), SnO_2, In_2O_3, and ZnO, on the semi-conductor film of a diode component. In drawing 1 , although current collection electrode 108D is not directly prepared on semi-conductor layer 104D of the diode component 102 but there is no Mitsuteru putting, the laminating of the transparent electrode 107D is carried out for the metal of current collection electrode 108D of a diode component.preventing invading into the semi-conductor film on the generation-of-electrical-energy electrical potential difference of a solar battery element, and preventing the short circuit of a diode component.

[0041] In this invention, since the semi-conductor layer of a solar battery element and the semi-conductor layer of a diode component consist of a homogeneous silicon system non-single crystal, they can be simultaneously formed on a conductive substrate. although the semi-conductor film of a solar battery element 101 and the diode component 102 is separated on the conductive substrate 103 in drawing 1 -- i type layer 105D of a diode component -- i type layer 105A of a solar battery element, simultaneously n(p) type layer 104D -- 104B, simultaneously transparence electric conduction film 107D -- 107, simultaneously current collection electrode 108D -- 108 -- simultaneously, deposition formation can be carried out. In that case, in order to make the part of a diode component deposit some deposition film of a solar battery element, well-known means, such as masking, can be used. In case film other than the required film is deposited with a diode component in a solar battery element, a diode component formation field can be covered with a mask, and only the desired film can be chosen and deposited by making it the film not accumulate.

[0042] ((b) Solar battery) Drawing 2 is the typical sectional view showing an example of the solar battery concerning this invention, and calls a solar battery b henceforth. A solar battery b is the case where the semi-conductor film deposited as a diode component is deposited continuously, without dissociating with a solar battery element.

[0043] 201-210 in drawing 2 support 101-110 of drawing 1 . drawing 2 -- setting -- i type of the diode component 202 -- layer 205A and n(p) type layer 204B -- i type of a solar battery element 201 -- layer 205A and n(p) type layer 204B are followed.

[0044] Although the leakage current arises in a longitudinal direction in this semi-conductor layer by sharing a semi-conductor layer, the resistivity of the non-single-crystal-silicon film is quite high, since thickness is also thin, the leakage current to the longitudinal direction in this semi-conductor layer is very small, and if even the high transparent electrode and current collection electrode of conductivity are separated about several mm, it will not have an adverse effect on the property of a solar battery element practically. Although a level difference is made at the edge of a solar

battery element 201 in the semi-conductor layer to share, even if it is [spacing of a solar battery element and a diode component] narrower for the film not to continue here and to be cut with the level difference, it is more desirable at the point that the lateral leakage current can be prevented.

[0045] In addition, when light is irradiated, since the photoelectromotive force of hard flow is generated, although there is no up electrode and a current is hardly collected, it is desirable [the field between a solar battery element and a diode component / a solar battery element] to apply protection-from-light coating 210 grade, and to shade.

[0046] ((c) Solar battery) Drawing 3 is the typical sectional view showing an example of the solar battery concerning this invention, and calls a solar battery c henceforth. A solar battery c is the case where a solar battery element and a diode component are prepared through a conductive substrate. 301-309 in drawing 3 support 101-109 of drawing 1 .

[0047] In this case, since the diode component 302 is formed in the optical exposure rear face of the conductive substrate 301, the light-receiving area of a solar cell module does not decrease by formation of a diode component. Moreover, it is possible not to care about reduction of light-receiving area, but to form a diode component in a large area, and the large current capacity of a diode component can be taken. Furthermore, since a diode component is shaded by the conductive substrate, there is an advantage that it is not necessary to shade a diode component in protection-from-light coatings etc.

[0048] In addition, the semi-conductor layers 305D and 304D of the diode component 302 can be easily formed in this case by depositing the semi-conductor film also on the rear face of the conductive substrate 303 simultaneously at the time of deposition of the semi-conductor layers 305A and 304B of a solar battery element 301.

[0049] Moreover, in drawing 3 , although the diode component is formed only in the rear face of a conductive substrate, it may be formed in both sides of a rear face and a front face.

[0050] ((d) Solar battery) Drawing 4 is the typical sectional view showing an example of the solar battery concerning this invention, and calls a solar battery d henceforth. A solar battery d is the case where carried out parallel connection of the diode 411 which becomes the solar battery a of drawing 1 from a single crystal semiconductor further, and it is formed. 401-409 in drawing 4 support 101-109 of drawing 1 .

[0051] As mentioned above, when the diode component 402 is formed on the same machine hill 403 at a solar battery element 401, parallel connection is carried out to hard flow with lead wire 409 and a solar-battery array is formed, even if there is no single crystal diode 411, it acts as a by-pass diode.

[0052] At this time, since the forward voltage of the diode component 402 is low, even if partial optical cutoff arises in a solar-battery array, the reverse voltage impressed to a solar battery element 401 becomes quite low.

[0053] However, the diode component 402 is on the same substrate 403 as a solar battery element 401, and in order to prevent reduction of light-receiving area, as compared with a solar battery element 401, the area of the diode component 402 cannot do it not much greatly. Therefore, when there is no single.crystal diode 411 and partial optical cutoff arises in a solar-battery array, the generating current of other solar battery elements of a solar-battery array almost equal to the small diode component 402 on the generating current of a solar battery element 401 will flow as forward current, and when the allowable-current capacity of the diode component 402 which this forward current becomes from a silicon system non-single crystal semiconductor is exceeded, there is a danger of being destroyed diode component 402.

[0054] When the single crystal diode 411 also with big [current capacity] forward voltage being also high is connected to the diode component 402 in this direction at juxtaposition, the high current in the field where applied voltage is high flows the single crystal diode 411, the small current in the field where applied voltage is lower than the forward voltage of single crystal diode acts so that the diode component 402 which consists of a non-single crystal semiconductor may be flowed, and reduction in the forward voltage of a by-pass diode and coexistence of buildup of allowable-current capacity are achieved.

[0055] In addition, the diode component according to individual which consists of silicon or germanium and has pn junction, a pin junction, or Schottky barrier junction structure as single crystal diode used in this invention is **********. the forward direction allowable-current capacity (maximum rating value) of this single crystal diode -- desirable -- the short-circuit current at the time of AM1.5 (1000 W/m2) exposure of each solar battery element -- it takes more preferably for 3 or more times more than twice.

[0056] (Solar-battery e-h) Drawing 6 - drawing 9 are the typical sectional views showing an example of the solar battery concerning this invention, and call solar-battery e-h henceforth. Solar-battery e-h is the case where the three-layer tandem-die solar battery element which carried out the three-piece laminating of nip or the pin junction is used.

[0057] In this case, two or more combination by in which semi-conductor layer and coincidence of a solar battery element the semi-conductor layer used for the diode component formed on the same substrate as a solar battery element is formed exists.

[0058] Drawing 6 - drawing 9 have shown the semi-conductor layer continuously so that it may turn out the semi-

conductor layer [which semi-conductor layer of a solar battery element, and] of a diode component were formed simultaneously.

[0059] Drawing 6 (solar battery e) is the case where the semi-conductor layer of a diode component is used as the i-type semiconductor layer of the cel of the 1st layer of a solar battery element, and n (or p) mold semi-conductor layer of the cel of the 2nd layer from the bottom at order.

[0060] Drawing 7 (solar battery f) is the case where the semi-conductor layer of a diode component is used as the i-type semiconductor layer of the cel of the 2nd layer of a solar battery element, and n (or p) mold semi-conductor layer of the cel of the 3rd layer from the bottom at order.

[0061] Drawing 8 (solar battery g) is the case where the semi-conductor layer of a diode component is used as the i-type semiconductor layer of the cel of the 1st layer of a solar battery element, n (or p) mold semi-conductor layer of the cel of the 2nd layer, and n (or p) mold semi-conductor layer of the cel of the 3rd layer from the bottom at order.

[0062] In this case, thickness of the impurity dope layer of a diode component can be thickened.

[0063] Drawing 9 (solar battery h) is the case where the semi-conductor layer of a diode component is used as the i-type semiconductor layer of the cel of the 1st layer of a solar battery element, the i-type semiconductor layer of the cel of the 2nd layer, and n (or p) mold semi-conductor layer of the cel of the 2nd layer from the bottom at order. In this case, a diode component can make substantial thickly thickness of a genuineness i-type semiconductor layer.

[0064] (Diode component) As thickness of a genuineness semi-conductor layer, the range of about 50 to about 500nm is substantially [the diode component concerning this invention] desirable. In less than about 50nm, it is easy to produce a pinhole in a semi-conductor layer, and easy to produce dielectric breakdown. Moreover, if thicker than about 500nm, the electric field inside this layer will become weaker, and lowering of diode characteristics will be caused.

[0065] Moreover, as thickness of the impurity dope layer substantially joined to the genuineness semi-conductor film with the diode component concerning this invention, it is desirable that it is about 5nm or more. In less than about 5nm, it is difficult to form a semi-conductor layer in homogeneity, and it causes lowering of diode characteristics.

[0066] (Conductive substrate) As a conductive substrate concerning this invention, there are little deformation and distortion in the temperature needed at the time of semi-conductor film formation, and it is desirable that it is what has desired reinforcement and has good conductivity. Specifically, what performed electric conduction processing with vacuum deposition, the sputtering method, plating, etc. is mentioned to front faces, such as heat resistant resin, such as metal plates, such as a stainless steel, aluminum and its alloy, iron and its alloy, copper, and its alloy, or polyimide, a polyamide, polyethylene terephthalate, and epoxy, and a glass plate, in a metal simple substance or an alloy, a transparent conductive oxide, etc.

[0067] in addition, the long wave which reached the conductive substrate at the substrate -- a metal layer of a different kind for the object, such as improvement in the reflection factor of light, prevention of the counter diffusion of a substrate ingredient and a semi-conductor layer, improvement in adhesion, and smoothing of a substrate front face, may be prepared in a semi-conductor stratification side front face.

[0068] When preparing as a light reflex layer, as such a metal layer, the metal with a high reflection factor is suitable by near-infrared from the lights, such as Ag, aluminum, Cu, Au, and AlSi.

[0069] Moreover, when these metal layers are prepared, it is desirable to prepare a transparence conductive layer among these metal layers and semi-conductor layers, in order to prevent diffusion of the metal of semi-conductor layer HE from a metal layer.

[0070] As such a transparence conductive layer, transparent conductive oxides, such as ZnO, SnO2, In2O3, and ITO, are mentioned as optimal thing.

[0071] (The manufacturing installation and the manufacture approach of a silicon system non-single crystal half conductor layer) In forming a silicon system non-single crystal half conductor layer, in the solar battery concerning this invention, it is possible to use various kinds of manufacture approaches and a manufacturing installation.

[0072] The solar battery shown in drawing 1 is producible using the manufacturing installation of a configuration of having been shown in drawing 10 . The manufacturing installation shown in drawing 10 is the so-called continuation manufacturing installation of the roll two roll method by the plasma CVD method. In drawing 10 , the sectional view which saw drawing 10 (A) from the longitudinal direction of equipment, and drawing 10 (B) are the sectional views seen from the upper part of this equipment.

[0073] In drawing 10 , a band-like conductive substrate begins to roll n according [1004A, 1005A, 1006A, 1004B, 1005B, and 1006B] to a plasma-CVD method, i, the membrane formation room of p (or p, i, n) type layer, and 1001 and 1002, and they are ** and a rolling-up room. The discharge room 1008 is established in the vacuum chamber of each membrane formation room, and deposition of the silicon system non-single crystal semiconductor film is performed by occurring glow discharge in the discharge indoor section. The vacuum chamber of each membrane formation room is connected by the gas gate 1007 which passes purge gas, such as helium, to a slit and prevents mutual

mixing of the gas between membrane formation rooms. 1003 is a band-like conductive substrate like a stainless steel sheet with 0.13mm [in thickness], and a width of face of 36cm. It passes through six membrane formation rooms 1004A, 1005A, 1006A, 1004B, 1005B, and 1006B, beginning to be wound and being continuously conveyed from the supply room 1001. While being rolled round by the rolling-up room 1002, the cascade screen of the silicon system non-single crystal semiconductor for the solar battery elements of two-layer nip (or pin) structure to the field of the conductive substrate other side of drawing 10 (B) to the front face The cascade screen of the silicon system non-single crystal semiconductor for the diode components of in (or ip) structure is formed in the field of the conductive substrate near side of drawing 10 (B).

[0074] In addition, temperature control means, such as a heating heater which controls a substrate at each membrane formation room to the predetermined temperature for which it was suitable at deposition of a semi-conductor although not shown in drawing, A material gas installation means to introduce the material gas for semi-conductor formation into each membrane formation interior of a room from a gas supply means, The non-illustrated exhaust pipe which exhausts a membrane formation room with an exhaust air means, and is adjusted to a predetermined pressure, A discharge means by which it does not illustrate [which supplies high-frequency power to the gas of the membrane formation interior of a room from a non-illustrated RF generator] is established. At the membrane formation rooms 1004A, 1005A, 1006A, 1004B, 1005B, and 1006B, n, i, p, n, i, and the silicon system non-single crystal half conductor layer of p (or p, i, n, p, i, n) mold deposit by the plasma-CVD method at each discharge room 1008, respectively.

[0075] A mask 1009 is formed in the discharge room 1008 upper parts between the conductive substrates 1003, and a desired semi-conductor layer deposits on the position on the band-like conductive substrate 1003.

[0076] Opening of a mask 1009 is in the location of each discharge room 1008 throats, and it is shown in drawing 10 (B) whether a semi-conductor layer deposits in which location. It separates into the semi-conductor stratification field 1010 for solar battery elements of the other side of this drawing conductivity substrate 1003, and the semi-conductor film formation field 1011 for diode components of a near side, and the semi-conductor cascade screen for the diode components of in (or ip) structure deposits [the semi-conductor cascade screen for the solar battery elements of nipnip (or pinpin) structure] opening of a mask 1009 on the other side of this drawing conductivity substrate 1003 at a near side.

[0077] If such equipment is used, the semi-conductor layer of the solar battery of this invention can be formed. Then, the transparence electric conduction film of ITO and SnO2 grade can be formed by the well-known vacuum deposition method or the sputtering method, current collection electrodes, such as Ag and aluminum, can be further formed with a vacuum deposition method, screen printing, etc., the current collection electrode of a solar battery element and a diode component can be connected with lead wire, and the solar battery of this invention as shown in drawing 1 can be manufactured by applying a black protection-from-light coating etc. on a diode component.

[0078] (Solar cell module) The solar cell module concerning this invention carries out the series connection of two or more solar batteries which connected the by-pass diode component to the solar battery element mentioned above, and points out what carried out the modularization.

[0079] If one solar battery becomes a shadow in n solar batteries by which the series connection was carried out when there is no by-pass diode, since open circuit voltage twice (n-1) the reverse voltage [max and] of other solar battery elements will be impressed to the solar battery which became a shadow, when a partial shadow is made, the number of series connections can be increased only within limits to which the reverse voltage concerning a solar battery element does not exceed pressure-proofing of a solar battery element.

[0080] However, the number of series connections of the solar battery at the time of the modularization of the solar battery of this invention being carried out since the by-pass diode is connected for every solar battery element can be freely set as the appearance from which desired output voltage is obtained.

[0081] Moreover, it may be made to carry out parallel connection to two or more solar batteries by which did not necessarily need to connect the diode which consists of a single crystal semiconductor when carrying out the series connection of the solar battery and carrying out a modularization, although parallel connection of the diode which becomes the by-pass diode component which consists of a silicon system non-single crystal semiconductor in this invention from a single crystal semiconductor may be carried out further for every solar battery, and the series connection was carried out at a rate of one piece.

[0082] Furthermore, when carrying out the series connection of two or more solar cell modules, you may make it put only one diode which consists of a single crystal semiconductor into the solar cell module of one sheet.

[0083]

[Example] Below, although the solar battery and solar cell module of this invention are explained in full detail, this invention is not limited at all by these examples.

[0084] (Example 1) In this example, the semi-conductor film of the solar battery element of the nipnip structure which

consists of a silicon system non-single crystal semiconductor, and the diode component of in structure which consists of a silicon system non-single crystal semiconductor was continuously formed on the conductive substrate using the manufacturing installation of a configuration of having been shown in drawing 10 , and the solar battery of a configuration of having been shown in drawing 1 was produced.

[0085] Below, the production approach is explained according to a procedure.

(1) Where it wound the 1000nm ZnO transparence conductive layer around formation and the band-like conductive substrate 1003 which carried out the laminating is wound around a coiled form as 500nm Ag layer and a diffusion prevention layer of Ag as a rear-face reflecting layer by the DC magnetron sputtering method well-known on the front face of the band-like stainless plate made from SUS430BA (0.13mm in width-of-face [of 356mm] x die-length [of 200m] x thickness), it set to substrate volume ****** 1001. Next, the membrane formation rooms 1004A, 1005A, 1006A, 1004B, 1005B, and 1006B were made to penetrate this conductive machine hill 1003 through each gas gate 1007, and tension was applied to delivery and extent not slackening to the substrate rolling-up room 1003.

[0086] In addition, the non-illustrated bobbin with which the **** film made of aramid paper (0.05mm in width-of-face [of 356mm] x die-length [of 200m] x thickness) dried enough was twisted around the substrate **** picking room 1003 is set, and this protection film was involved in with the conductive machine hill 1003 where the semi-conductor layer was formed in the front face.

[0087] (2) After setting a conductive substrate, having carried out evacuation of the inside of each membrane formation room 1004A-1006B once, and exhausting it succeedingly with a non-illustrated evacuation pump, helium gas was introduced and each membrane formation indoor section was made into about 350 degrees C the ******-king in about 200Pa helium ambient atmosphere.

[0088] (3) After heating baking, exhausting each ** 1004A-1006B with an evacuation pump, respectively, H2 was carried out at each gas gate, and predetermined flow rate installation of each material gas was carried out as gate gas at the discharge room 1008 of 1000 sccm(s) each and each membrane formation room. And by adjusting the opening of the throttle valve which is not illustrated [which was prepared in the exhaust pipe between the evacuation pump which exhausts each membrane formation room, and each membrane formation room], the interior of substrate volume ****** 1001 and the substrate rolling-up room 1002 was set to 130Pa, and setting pressure of each discharge indoor section of each membrane formation rooms 1004A-1006B was set to 135Pa.

[0089] (4) In the place by which the pressure of each ** was stabilized, the rolling-up bobbin of the conductive substrate 1003 of the substrate rolling-up room 1002 was rotated, and the conductive substrate 1003 was moved in the direction which goes to membrane formation room 1006B from membrane formation room 1004A at the rate of 250 mm/min. Moreover, temperature control was performed so that the conductive substrate which moves might become temperature predetermined at each discharge room.with a temperature control.means formed in each.discharge room. 1008 by which it does not illustrate.

[0090] (5) High-frequency power was switched on through matching equipment from the non-illustrated RF generator, glow discharge decomposition of the material gas of each discharge interior of a room was carried out, and the discharge electrode which is not illustrated [which was prepared in each discharge room of the membrane formation rooms 1004A-1006B] was made to generate the plasma in the place by which the temperature of a substrate was stabilized. According to the membrane formation conditions shown in a table 1, deposition of the semi-conductor film was performed on the conductive substrate which moves continuously in each membrane formation interior of a room, spacing of 6mm was opened on the conductive substrate which is width of face of 356mm, and the two-layer tandem-die solar battery element of nipnip structure with a width of face of 300mm and the diode component of in structure with a width of face of 50mm were formed.

[0091] (6) After carrying out deposition formation of the semi-conductor film over about 170m of a band-like substrate, the charge of discharge power, installation of material gas, and heating of a conductive substrate and a membrane formation room were suspended, the purge of the membrane formation interior of a room was performed, after cooling a conductive substrate and the interior of equipment enough, equipment was opened, and the conductive substrate which the semi-conductor layer was formed in the front face, and was wound around the coiled form was picked out from equipment.

[0092] (7) On the formed semi-conductor film, the ITO thin film of 70nm of thickness was formed as transparence electric conduction film by the sputtering method, and thin line-like Ag electrode was formed in fixed spacing as a current collection electrode with the screen printing using Ag ** 1 strike. In addition, the transparence electric conduction film and a current collection electrode were formed only on the semi-conductor film, and connected the current collection electrode on a solar battery element, and the current collection electrode on a diode component with the lead wire of a thin copper plate.

[0093] (8) After applying the black coating for protection from light to the part of a diode component, the conductive

substrate in which the solar battery was formed was cut for every die length of 100mm, and 150 solar batteries with a width of face [of 356mm] and a die length of 100mm were produced. Drawing 1 is the typical sectional view showing the lamination of the produced solar battery.

[0094] (9) This solar battery was put through fat-proof [EVA] with a thickness of about 0.5mm (ethylene vinyl acetate) between the fluorine system surface-protection sheet [the copolymer ETFE of ethylene tetrafluoride and ethylene (E. I. du Pont de Nemours tefzel)] with a thickness of 0.1mm, and the zinc paint steel plate with a thickness of 0.3mm, and it closed by resin by carrying out heating compression using well-known vacuum lamination equipment.

[0095] (10) The above-mentioned process (1) The place which investigated the current-voltage characteristic of the solar battery produced by - (9), Also where the diode component was operating as a by-pass diode and light is intercepted in reverse voltage 0.3V, it is the same as the short-circuit current at the time of AM1.5 (1000 W/m2) exposure of a solar battery element -- it was checked that only very low reverse voltage is impressed to a solar battery element even if the current of ** flows and it impresses an electrical potential difference to hard flow in the state of dark.

[0096] (11) Light was thoroughly intercepted to the produced solar battery, the constant voltage power supply of 1V was connected to hard flow, it put into environmental-test equipment with a% [of humidity] of 95, and a temperature of 50 degrees C, partial protection from light was performed under highly humid, and the durability test reproducing the condition that reverse voltage was impressed was performed continuously for 1 hour. In addition, when a current-limiting circuit was established in a constant voltage power supply and the current beyond the short-circuit current at the time of AM1.5 (1000 W/m2) exposure of a solar battery element flowed, it was made to operate as a constant current power supply of the short-circuit current at the time of AM1.5 (1000 W/m2) exposure of a solar battery element.

[0097] Consequently, as for the parallel resistance of the solar battery in the humidity of 50%, the temperature of 25 degrees C, and a dark condition, it turned out that the average before a trial be maintain at the level which a problem do not have in any way practically although 100komegacm2 and lowering be saw for the average after 10 - M omegacm2 and a trial before and after the durability test, and there be no almost change in the curvilinear factor of a solar battery element, and open circuit voltage.

[0098] Moreover, the photoelectric conversion efficiency at the time of AM1.5 (1000 W/m2) exposure at the humidity of 50% of the solar battery after a durability test and the temperature of 25 degrees C was hardly changing with an average of 95% of value before a trial.

[0099] (Example 1 of a comparison) In case a solar battery is produced using the equipment of drawing 10 , this example closes the opening 1011 for diode components of the mask of each discharge room, and the point it was made not to deposit the semi-conductor film for diode components differs from an example 1 by it.

[0100] The solar battery of this example consists of a part of the solar battery element 101 of drawing 1 , and does not have a diode component. Therefore, spreading of the protection-from-light coating 110 or the connection of lead wire 109 which were indicated in the example 1 were not performed.

[0101] Thus, the produced solar battery was closed by resin by the example 1 and these conditions, partial protection from light was performed under highly humid on an example 1 and these conditions, and the durability test reproducing the condition that reverse voltage was impressed was performed continuously for 1 hour.

[0102] Consequently, before and after the durability test, the average after 10-M omegacm2 and a trial is [the average before a trial] as large as 1komegacm2, the parallel resistance of the solar battery in the humidity of 50%, the temperature of 25 degrees C, and a dark condition was falling, effect appeared in the current-voltage curve of a solar battery element, and a curvilinear factor and open circuit voltage fell greatly.

[0103] Moreover, the photoelectric conversion efficiency at the time of AM1.5 (1000 W/m2) exposure at the humidity of 50% of the solar battery after a durability test and the temperature of 25 degrees C fell to an average of 70% of value before a trial.

[0104] In addition, the photoelectric conversion efficiency before the durability test of the solar battery element which does not connect a diode component was completely the same as the photoelectric conversion efficiency before the durability test of the solar battery which connected the diode component of an example 1, and it was checked by connection of a diode component in the example 1 that there had been no effect in the photoelectric conversion efficiency of a solar battery element.

[0105] (Example 2) In this example, the point which produced the solar battery of a configuration of having been shown in drawing 1 differs from an example 1 using the manufacturing installation of a configuration of having been shown in drawing 10 by making into reversed polarity the conductivity type of the semi-conductor film which forms membranes at the membrane formation rooms 1004A, 1006A, 1004B, and 1006B.

[0106] That is, the semi-conductor film of the solar battery element of the pinpin structure which consists of a silicon

system non-single crystal semiconductor, and the diode component of ip structure which consists of a silicon system non-single crystal semiconductor was continuously formed on the conductive substrate. A table 2 is the production conditions of the semi-conductor film in each membrane formation room.
[0107] Thus, the produced solar battery was closed by resin by the example 1 and these conditions, partial protection from light was performed under highly humid on an example 1 and these conditions, and the durability test reproducing the condition that reverse voltage was impressed was performed continuously for 1 hour.
[0108] Consequently, as for the parallel resistance of the solar battery in the humidity of 50%, the temperature of 25 degrees C, and a dark condition, the average before a trial is maintained at the level which a problem does not have in any way practically although 100komegacm2 and lowering were seen for the average after 10-M omegacm2 and a trial before and after the durability test, and there was almost no change in the curvilinear factor of a solar battery element, and open circuit voltage.
[0109] Moreover, the photoelectric conversion efficiency at the time of AM1.5 (1000 W/m2) exposure at the humidity of 50% of the solar battery after a durability test and the temperature of 25 degrees C was hardly changing with an average of 95% of value before a trial.
[0110] (Example 3) In this example, parallel connection of the diode which becomes the diode component of in structure which consists of a silicon system non-single crystal semiconductor from single crystal silicon is carried out, and the point which produced the solar battery of a configuration of having been shown in drawing 4 differs from an example 1.
[0111] Below, the production approach is explained according to a procedure.
(1) The semi-conductor film of the solar battery element of the nipnip structure which consists of a silicon system non-single crystal semiconductor, and the diode component of in structure which consists of a silicon system non-single crystal semiconductor was continuously formed on the conductive substrate like the example 1 using the manufacturing installation of a configuration of having been shown in drawing 10 .
[0112] (2) the maximum rating of forward current -- 3 times of the short-circuit current at the time of AM1.5 (1000W/m2) exposure of a solar battery element -- forward voltage when forward current is equal to the short-circuit current at the time of AM1.5 (1000 W/m2) exposure of a solar battery element -- about 0.8 -- parallel connection of the diode which consists of single crystal silicon which is V was carried out through lead wire, and the solar battery of a configuration of having been shown in drawing 4 was manufactured.
[0113] In addition, the forward direction carried out parallel connection to it, as the diode which consists of a diode component which consists of a silicon system non-single crystal semiconductor, and single crystal silicon became the same direction.
[0114] Thus, the produced solar battery was closed by resin by the example 1 and these conditions, partial protection from light was performed under highly humid on an example 1 and these conditions, and the durability test reproducing the condition that reverse voltage was impressed was performed continuously for 1 hour.
[0115] Consequently, as for the parallel resistance of the solar battery in the humidity of 50%, the temperature of 25 degrees C, and a dark condition, the average before a trial is maintained at the level which a problem does not have in any way practically although 50komegacm2 and lowering were seen for the average after 5-M omegacm2 and a trial before and after the durability test, and there was almost no change in the curvilinear factor of a solar battery element, and open circuit voltage.
[0116] Moreover, the photoelectric conversion efficiency at the time of AM1.5 (1000 W/m2) exposure at the humidity of 50% of the solar battery after a durability test and the temperature of 25 degrees C was hardly changing with an average of 95% of value before a trial.
[0117] (Example 4) In this example, the partial change of the manufacturing installation of a configuration of having been shown in drawing 10 is carried out, and opening of the mask 1009 of the discharge room 1008 is not divided into two places at each membrane formation rooms 1005A and 1004B, but the point which produced the solar battery of a configuration of that the semi-conductor film formation field 1010 for solar battery elements showed the semi-conductor film formation field 1011 for diode components to drawing 2 continuously as differs from an example 1.
[0118] That is, the semi-conductor film of the solar battery element of the nipnip structure which consists of a silicon system non-single crystal semiconductor, and the diode component of in structure which consists of a silicon system non-single crystal semiconductor was continuously formed on the conductive substrate.
[0119] Thus, the produced solar battery was closed by resin by the example 1 and these conditions, partial protection from light was performed under highly humid on an example 1 and these conditions, and the durability test reproducing the condition that reverse voltage was impressed was performed continuously for 1 hour.
[0120] Consequently, as for the parallel resistance of the solar battery in the humidity of 50%, the temperature of 25 degrees C, and a dark condition, the average before a trial is maintained at the level which a problem does not have in

any way practically although 100komegacm2 and lowering were seen for the average after 1-M omegacm2 and a trial before and after the durability test, and there was almost no change in the curvilinear factor of a solar battery element, and open circuit voltage.

[0121] Moreover, the photoelectric conversion efficiency at the time of AM1.5 (1000 W/m2) exposure at the humidity of 50% of the solar battery after a durability test and the temperature of 25 degrees C was hardly changing with an average of 95% of value before a trial.

[0122] (Example 5) In this example, as the partial change of the manufacturing installation of a configuration of having been shown in drawing 10 is carried out, the semi-conductor film for solar battery elements is formed in the side front of a conductive substrate by width of face of 350mm and the semi-conductor film for diode components is formed in the background of a conductive substrate by width of face of 150mm at each membrane formation rooms 1005A and 1004B, the point which produced the solar battery of a configuration of having been shown in drawing 3 differs from an example 1.

[0123] That is, the semi-conductor film of the solar battery element of the nipnip structure which becomes the front flesh side of a conductive substrate from a silicon system non-single crystal semiconductor, and the diode component of in structure which consists of a silicon system non-single crystal semiconductor was formed continuously.

[0124] In addition, the diode component was formed in the rear face of a conductive substrate, and since incident light was interrupted, spreading of a protection-from-light coating was not performed for a diode component.

[0125] Thus, the produced solar battery was closed by resin by the example 1 and these conditions, partial protection from light was performed under highly humid on an example 1 and these conditions, and the durability test reproducing the condition that reverse voltage was impressed was performed continuously for 1 hour.

[0126] Consequently, as for the parallel resistance of the solar battery in the humidity of 50%, the temperature of 25 degrees C, and a dark condition, the average before a trial is maintained at the level which a problem does not have in any way practically although 100komegacm2 and lowering were seen for the average after 1-M omegacm2 and a trial before and after the durability test, and there was almost no change in the curvilinear factor of a solar battery element, and open circuit voltage.

[0127] Moreover, the photoelectric conversion efficiency at the time of AM1.5 (1000 W/m2) exposure at the humidity of 50% of the solar battery after a durability test and the temperature of 25 degrees C was hardly changing with an average of 95% of value before a trial.

[0128] (Example 6) the manufacturing installation of a configuration of that this example showed to drawing 10 -- a partial change -- carrying out -- between membrane formation room 1006B and the substrate rolling-up rooms 1002 -- three more membrane formation rooms, n(p) type layer membrane formation room 1004C, and i type layer membrane formation room -- 1005C and p(n) type layer membrane.formation room 1006C were added.

[0129] As the semi-conductor film for the three-layer tandem-die solar battery elements of nipnipnip (or pinpinpin) structure is formed and the semi-conductor film for diode components is formed in some conductive substrates at the membrane formation rooms 1005A, 1005B, and 1004C by this, the point which produced the solar battery of a configuration of having been shown in drawing 5 differs from an example 1.

[0130] That is, the semi-conductor film of the solar battery element of the nipnipnip structure which consists of a silicon system non-single crystal semiconductor, and the diode component of in structure which consists of a silicon system non-single crystal semiconductor was continuously formed on the conductive substrate like the example 1 except having changed the membrane formation conditions of each membrane formation room, as shown in a table 3.

[0131] Thus, the produced solar battery was closed by resin by the example 1 and these conditions, partial protection from light was performed under highly humid on an example 1 and these conditions, and the durability test reproducing the condition that reverse voltage was impressed was performed continuously for 1 hour.

[0132] Consequently, as for the parallel resistance of the solar battery in the humidity of 50%, the temperature of 25 degrees C, and a dark condition, the average before a trial is maintained at the level which a problem does not have in any way practically although 100komegacm2 and lowering were seen for the average after 10-M omegacm2 and a trial before and after the durability test, and there was almost no change in the curvilinear factor of a solar battery element, and open circuit voltage.

[0133] Moreover, the photoelectric conversion efficiency at the time of AM1.5 (1000 W/m2) exposure at the humidity of 50% of the solar battery after a trial and the temperature of 25 degrees C was hardly changing with an average of 95% of value before a trial.

[0134] (Example 7) In this example, the ten-step series connection of the solar battery which consisted of a solar battery element produced in the example 6 and a diode component was carried out, and the solar cell module was produced.

[0135] in addition -- each solar battery -- the maximum rating of forward current -- 3 times of the short-circuit current

at the time of AM1.5 (1000 W/m2) exposure of a solar battery element -- forward voltage when forward current is equal to the short-circuit current at the time of AM1.5 (1000 W/m2) exposure of a solar battery element -- about 0.8 -- the diode which consists of single crystal silicon which is V was connected to juxtaposition.

[0136] Thus, the produced solar cell module was closed by resin by the example 1 and these conditions, only one piece was thoroughly shaded in the solar battery which carried out the ten - step series connection with the mask, and the constant voltage power supply of 3V was connected to hard flow, it put into environmental test equipment with a% [of humidity] of 95, and a temperature of 50 degrees C, partial protection from light was performed under highly humid, and the durability test reproducing the condition that reverse voltage was impressed was performed continuously for 1 hour.

[0137] In addition, when a current-limiting circuit was established in a constant voltage power supply and the current beyond the short-circuit current at the time of AM1.5 (1000 W/m2) exposure of a solar battery element flowed, it was made to operate as a constant current power supply of the short-circuit current at the time of AM1.5 (1000 W/m2) exposure of a solar battery element.

[0138] Consequently, as for the parallel resistance in the humidity of 50% of the solar battery which intercepted light before and after the durability test, the temperature of 25 degrees C, and a dark condition, the average before a trial is maintain at the level which a problem does not have in any way practically although 50komegacm2 and lowering were saw for the average after 5 - M omegacm2 and a trial, and there was almost no change in the curvilinear factor of a solar battery element, and open circuit voltage.

[0139] Moreover, the photoelectric conversion efficiency at the time of AM1.5 (1000 W/m2) exposure at the humidity of 50% of the solar cell module which removed the protection-from-light mask after a trial, and the temperature of 25 degrees C was hardly changing with an average of 95% of value before a trial.

[0140] (Example 2 of a comparison) In this example, the point which used the current collection electrode of a diode component as the solar cell module to which the diode component of in structure which consists of a silicon system non-single crystal semiconductor is not connected as the diode component which consists of a silicon system non-single crystal semiconductor is not connected to except for the lead wire linked to a solar battery element differs from an example 7 in the solar cell module produced in the example 6. In addition, the diode which becomes each solar battery to which the ten-step series connection of the solar cell module was carried out from single crystal silicon like an example 7 was connected to juxtaposition.

[0141] Thus, the produced solar cell module was closed by resin by the example 1 and these conditions, only one piece was thoroughly shaded in the solar battery which carried out the ten - step series connection with the mask, and the constant voltage power supply of 3V was connected to hard flow, it put into environmental test equipment with a% [of humidity] of 95, and a temperature of 50 degrees C, partial protection from light was performed under highly humid, and the durability test reproducing the condition that reverse voltage was impressed was performed continuously for 1 hour.

[0142] In addition, when a current-limiting circuit was established in a constant voltage power supply and the current beyond the short-circuit current at the time of AM1.5 (1000 W/m2) exposure of a solar battery element flowed, it was made to operate as a constant current power supply of the short-circuit current at the time of AM1.5 (1000 W/m2) exposure of a solar battery element.

[0143] Consequently, before and after the durability test, the average after 5-M omegacm2 and a trial is [the average before a trial] as large as 1komegacm2, the parallel resistance in the humidity of 50% of the solar battery which intercepted light, the temperature of 25 degrees C, and a dark condition was falling, effect appeared in the current-voltage curve of a solar battery element, and a curvilinear factor and open circuit voltage fell greatly.

[0144] Moreover, the photoelectric conversion efficiency at the time of AM1.5 (1000 W/m2) exposure at the humidity of 50% of the solar cell module after a trial and the temperature of 25 degrees C fell to an average of 70% of value before a trial.

[0145]

[A table 1]

成膜室		1004A	1005A	1006A
太陽電池素子用堆積膜		n型a－Si 40nm	i型a－SiGe 100nm	p型微結晶Si 10nm
ダイオード素子用堆積膜			i型a－SiGe 100nm	
放電室搬送方向長さ(cm)		25	50	25
原料ガス流量 (sccm)	SiH_4	15	140	3
	GeH_4		60	
	H_2	150	500	500
	PH_3	1		
	BF_3			0.5
圧力 (Pa)		135	135	135
放電電力 (W)		50	200	500
基板加熱温度 (℃)		300	300	200
成膜室		1004B	1005B	1006B
太陽電池素子用堆積膜		n型a－Si 20nm	i型a－Si 100nm	p型微結晶Si 10nm
ダイオード素子用堆積膜		n型a－Si 20nm		
放電室搬送方向長さ(cm)		25	50	25
原料ガス流量 (sccm)	SiH_4	10	200	3
	GeH_4			
	H_2	150	500	500
	PH_3	1		

	BF_3			0.1
圧力	(Pa)	135	135	135
放電電力	(W)	50	200	500
基板加熱温度	(℃)	300	200	200

[0146]
[A table 2]

成膜室		1004A	1005A	1006A
太陽電池素子用堆積膜		p型a－Si 40nm	i型a－SiGe 100nm	n型微結晶Si 10nm
ダイオード素子用堆積膜			i型a－SiGe 100nm	
放電室搬送方向長さ(cm)		25	50	25
原料ガス流量 (sccm)	SiH_4	15	140	3
	GeH_4		60	
	H_2	150	500	500
	PH_3			0.5
	BF_3	1		
圧力 (Pa)		135	135	135
放電電力 (W)		50	200	500
基板加熱温度 (℃)		300	300	200
成膜室		1004B	1005B	1006B
太陽電池素子用堆積膜		p型a－Si 20nm	i型a－Si 100nm	n型微結晶Si 10nm
ダイオード素子用堆積膜		p型a－Si 20nm		
放電室搬送方向長さ(cm)		25	50	25
原料ガス流量 (sccm)	SiH_4	10	200	3
	GeH_4			
	H_2	150	500	500
	PH_3			0.1

	BF_3	1		
圧力	(Pa)	135	135	135
放電電力	(W)	50	200	500
基板加熱温度	(℃)	300	200	200

[0147]
[A table 3]

成膜室		1004A	1005A	1006A
太陽電池素子用堆積膜		n型a－Si 40nm	i型a－SiGe 100nm	p型微結晶Si 10nm
ダイオード素子用堆積膜			i型a－SiGe 100nm	
放電室搬送方向長さ(cm)		25	50	25
原料ガス流量 (sccm)	SiH_4	15	140	3
	GeH_4		60	
	H_2	150	500	500
	PH_3	1		
	BF_3			0.5
圧力 (Pa)		135	135	135
放電電力 (W)		50	200	500
基板加熱温度 (℃)		300	300	200
成膜室		1004B	1005B	1006B
太陽電池素子用堆積膜		n型a－Si 20nm	i型a－SiGe 100nm	p型微結晶Si 10nm
ダイオード素子用堆積膜			i型a－SiGe 100nm	
放電室搬送方向長さ(cm)		25	50	25
原料ガス流量 (sccm)	SiH_4	10	160	3
	GeH_4		40	
	H_2	150	500	500
	PH_3	1		

	BF_3			0.5
圧力 (Pa)		135	135	135
放電電力 (W)		50	200	500
基板加熱温度 (℃)		250	250	200
成膜室		1004C	1005C	1006C
太陽電池素子用堆積膜		n型a－Si 20nm	i型a－Si 100nm	p型微結晶Si 10nm
ダイオード素子用堆積膜		n型a－Si 20nm		
放電室搬送方向長さ(cm)		25	50	25
原料ガス流量 (sccm)	SiH_4	10	200	3
	GeH_4			
	H_2	150	500	500
	PH_3	1		
	BF_3			0.1
圧力 (Pa)		135	135	135
放電電力 (W)		50	200	500
基板加熱温度 (℃)		200	200	200

[0148]
[Effect of the Invention] the solar battery which can boil markedly the dependability of a solar battery and a solar cell module, and can raise it is obtained without controlling generating of a short circuit of the solar cell module by the partial optical cutoff under high humidity, and reducing the engine performance of a solar battery, even if it uses metals, such as Ag, for a rear-face reflecting layer or a current collection electrode since the reverse voltage impressed to each solar battery is very low according to this invention even if a partial shadow arises in a solar cell module as explained above.
[0149] Moreover, according to this invention, without carrying out insulating processing of the front face on the same conductive substrate, a solar battery element and a by-pass diode component can be formed simultaneously, and a solar battery and a solar cell module excellent in productivity with a by-pass diode can be offered.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the typical sectional view showing an example of the solar battery concerning this invention.
[Drawing 2] It is the typical sectional view showing other examples of the solar battery concerning this invention.
[Drawing 3] It is the typical sectional view showing other examples of the solar battery concerning this invention.
[Drawing 4] It is the typical sectional view showing other examples of the solar battery concerning this invention.
[Drawing 5] It is the typical sectional view showing other examples of the solar battery concerning this invention.
[Drawing 6] It is the typical sectional view showing other examples of the solar battery concerning this invention.
[Drawing 7] It is the typical sectional view showing other examples of the solar battery concerning this invention.
[Drawing 8] It is the typical sectional view showing other examples of the solar battery concerning this invention.
[Drawing 9] It is the typical sectional view showing other examples of the solar battery concerning this invention.
[Drawing 10] It is the typical sectional view showing an example of the manufacturing installation used for production of the solar battery concerning this invention.
[Description of Notations]
101, 201, 301, 401, 501, 601, 701, 801, 901 solar battery elements,
102, 202, 302, 402, 502, 602, 702, 802, a 902 diode component,
103, 203, 303, 403, 503, 603, 703, 803, 903, 1003 Conductive machine hill,
104A, 204A, 304A, 404A, 504A, 604A, 704A, 804A, 904A, 104B, 204B, 304B, 404B, 504B, 604B, 704B, 804B, 904B, 504C, 604C, 704C, 804C, 904C, 104D, 304D, 404D, 504D n (or p) mold semi-conductor layer,
105A, 205A, 305A, 405A, 505A, 605A, 705A, 805A, 905A, 105B, 205B, 305B, 405B, 505B, 605B, 705B, 805B, 905B, 505C, 605C, 705C, 805C, 905C, 105D, 305D, 405D, 505D It is a genuineness semi-conductor layer substantially,
106A, 206A, 306A, 406A, 506A, 606A, 706A, 806A, 906A, 106B, 206B, 306B, 406B, 506B, 606B, 706B, 806B, 906B, 506C, 606C, 706C, 806C, 906C p (or n) mold semi-conductor layer,
107, 207, 307, 407, 507, 607, 707, 807, 907, 107D, 207D, 307D, 407D, 507D, 607D, 707D, 807D, 907D Transparence electric conduction film,
108, 208, 308, 408, 508, 608, 708, 808, 908, 108D, 208D, 308D, 408D, 508D, 608D, 708D, 808D, 908D Current collection electrode,
109, 209, 309, 409, 509, 609, 709, 809, 909 lead wire,
110, 210, 410, 510, 610, 710, 810, 910 Protection-from-light coating,
411 Diode Which Consists of a Single Crystal Semiconductor,
1001 Substrate Volume ******,
1002 Substrate Rolling-Up Room,
1004A, 1004B n (or p) mold semi-conductor layer membrane formation room,
1005A, 1005B It is the genuineness membrane formation room of a semi-conductor layer substantially,
1006A, 1006B p (or n) mold semi-conductor layer membrane formation room,
1007 Gas Gate,
1008 Discharge Room,
1009 Mask,
1010 Semi-conductor Film Formation Field for Solar Battery Elements,
1011 The semi-conductor film formation field for diode components.

[Translation done.]